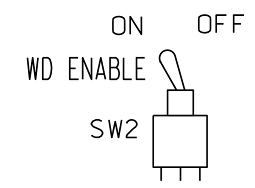
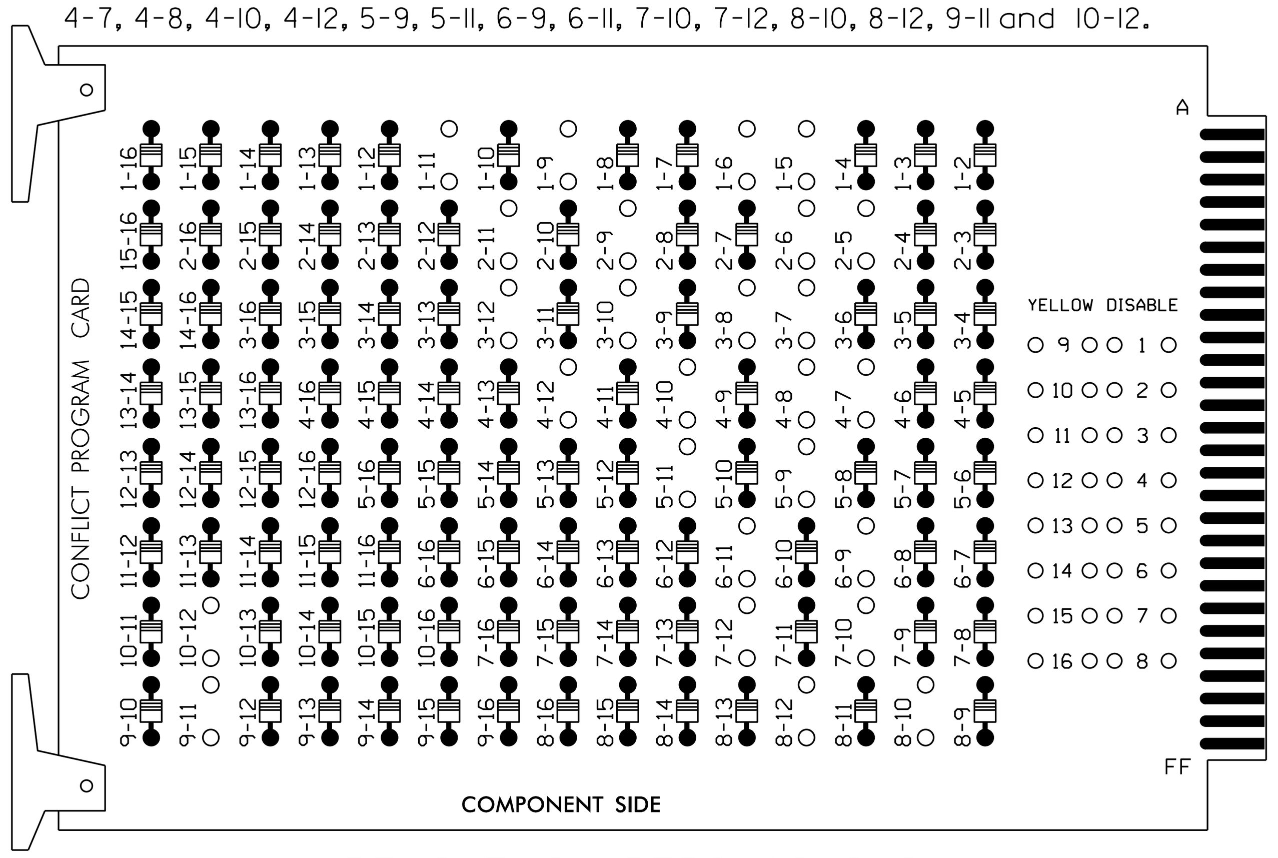
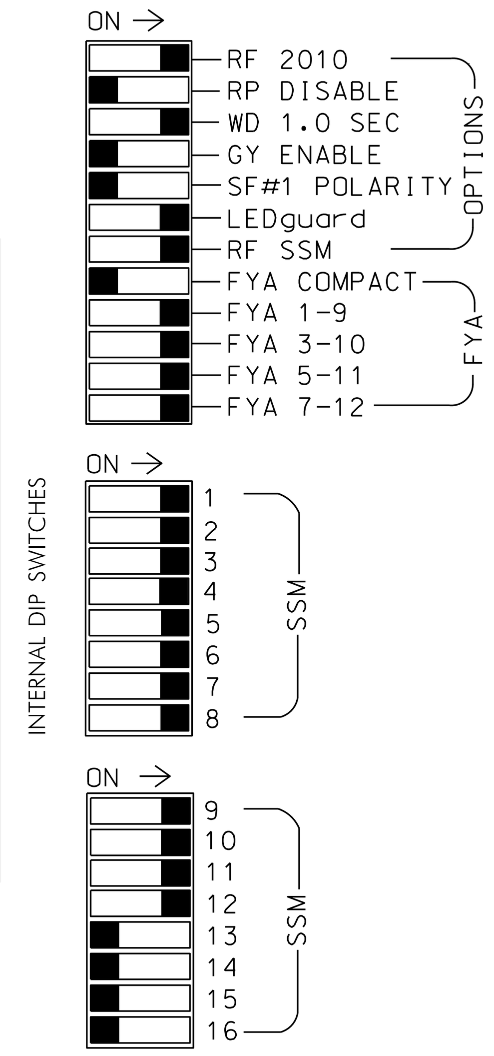
EDI MODEL 2010ECL-NC CONFLICT MONITOR PROGRAMMING DETAIL

(remove jumpers and set switches as shown)



REMOVE DIODE JUMPERS 1-5, 1-6, 1-9, 1-11, 2-5, 2-6, 2-9, 2-11, 3-7, 3-8, 3-10, 3-12, 4-7, 4-8, 4-10, 4-12, 5-9, 5-11, 6-9, 6-11, 7-10, 7-12, 8-10, 8-12, 9-11 and 10-12.





REMOVE JUMPERS AS SHOWN

■ = DENOTES POSITION OF SWITCH

NOTES:

1. Card is provided with all diode jumpers in place. Removal of any jumper allows its channels to run concurrently.
2. Make sure jumpers SEL2-SEL5 are present on the monitor board.

NOTES

1. To prevent "flash-conflict" problems, insert red flash program blocks for all unused vehicle load switches in the output file. The installer shall verify that signal heads flash in accordance with the Signal Plans.
2. Ensure that Red Enable is active at all times during normal operation. To prevent Red Failures on unused monitor channels, tie unused red monitor inputs 13,14,15 & 16 to load switch AC+ per the cabinet manufacturer's instructions.
3. Program phases 4 and 8 for Dual Entry.
4. Enable Simultaneous Gap-Out for all phases.
5. Program phases 2 and 6 for Variable Initial and Gap Reduction.
6. Program phases 2 and 6 for Start Up In Green.
7. Program phases 2 and 6 for Yellow Flash, and overlaps 1 and 2 as Wag Overlaps.

EQUIPMENT INFORMATION

CONTROLLER.............2070L
CABINET................332 /W/ AUX
SOFTWARE...............ECONOLITE OASIS
CABINET MOUNT..........BASE
OUTPUT FILE POSITIONS...18 WITH AUX. OUTPUT FILE
LOAD SWITCHES USED......S1,S2,S3,S4,S5,S6,S7,S8,S9,S10,S12,S13.
PHASES USED............1,2,3,4,5,6,7,8.
OVERLAP "A"............1+2
OVERLAP "B"............3+4
OVERLAP "C"............5+6
OVERLAP "D"............7+8

SIGNAL HEAD HOOK-UP CHART

LOAD SWITCH NO.	S1		S2	S2P	S3		S4	S4P	S5		S6	S6P	S7		S8	S8P	S9	S10	S11	S12	S13	S14
PHASE	1		2	2 PED	3		4	4 PED	5		6	6 PED	7		8	8 PED	OLA	OLB	SPARE	OLC	OLD	SPARE
SIGNAL HEAD NO.	11★	82	21,22	NU	31★	22	41,42	NU	51★	42	61,62	NU	71★	62	81,82	NU	11★	31★	NU	51★	71★	NU
RED	✳		128		✳		101		✳		134		✳		107							
YELLOW			129				102				135				108							
GREEN			130				103				136				109							
RED ARROW																	A121	A124		A114	A101	
YELLOW ARROW		126				117				132				123			A122	A125		A115	A102	
FLASHING YELLOW ARROW																	A123	A126		A116	A103	
GREEN ARROW	127	127			118	118			133	133			124	124								

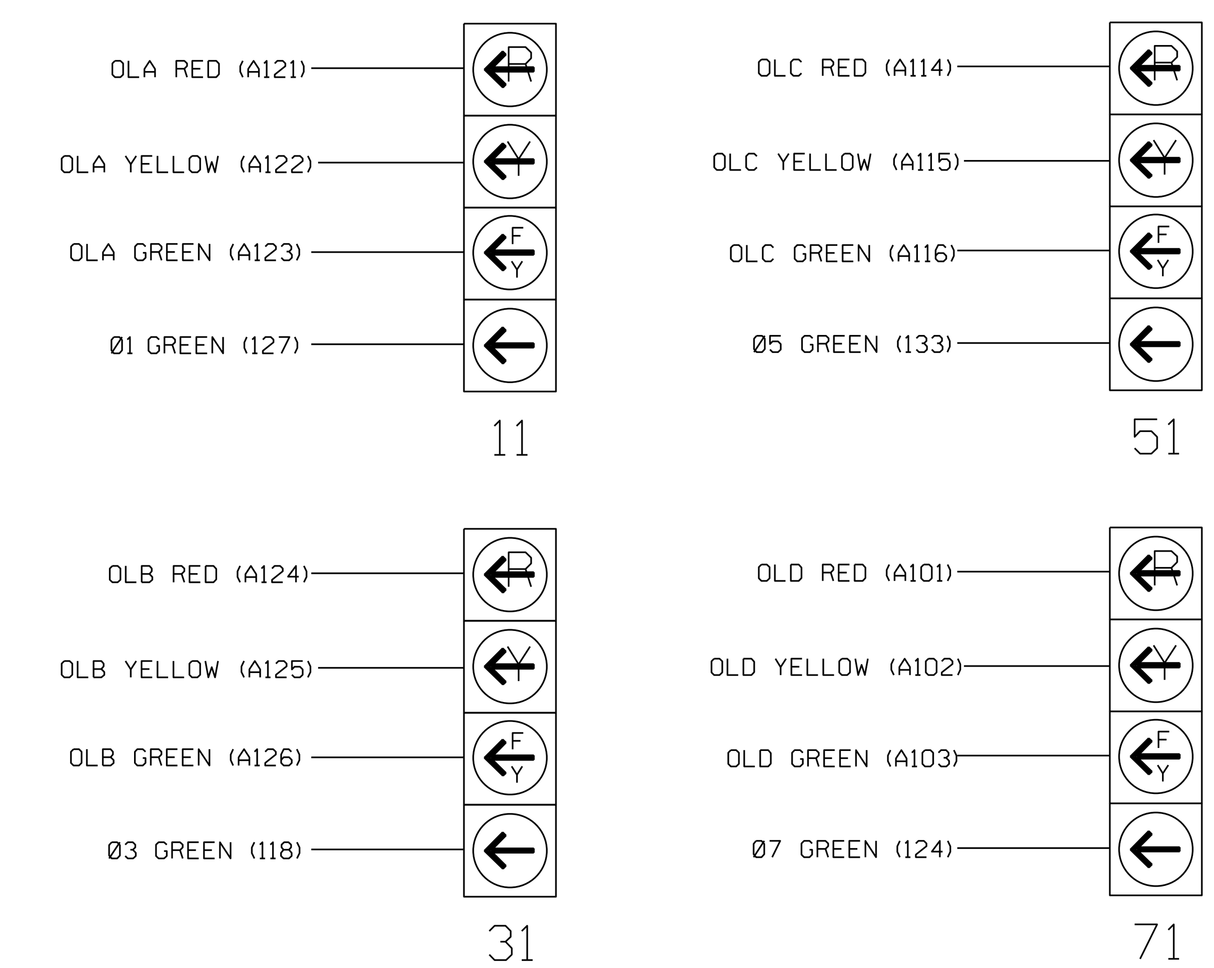
NU = Not Used

✳ Denotes install load resistor. See load resistor installation detail this sheet.

★ See pictorial of head wiring in detail below.

4 SECTION FYA PPLT SIGNAL WIRING DETAIL

(wire signal heads as shown)



NOTE

1. The sequence display for these signals require special logic programming. See sheet 2 of 7 for programming instructions.

INPUT FILE POSITION LAYOUT

(front view)

FILE		1	2	3	4	5	6	7	8	9	10	11	12	13	14
FILE "I"	U	Ø 1 1A	Ø 2 2A	SLOT EMPTY	WIRED INPUT ⊗	Ø 3 3A	Ø 4 4A	SLOT EMPTY	WIRED INPUT ⊗	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	FS DC ISOLATOR
	L	NOT USED	Ø 1 1B			NOT USED	Ø 4 4B								ST DC ISOLATOR
FILE "J"	U	Ø 5 5A	Ø 6 6A	SLOT EMPTY	WIRED INPUT ⊗	Ø 7 7A	Ø 8 8A	SLOT EMPTY	WIRED INPUT ⊗	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY	SLOT EMPTY
	L	NOT USED	Ø 5 5B			NOT USED	Ø 8 8B								

EX.: 1A, 2A, ETC. = LOOP NO.'S

FS = FLASH SENSE
ST = STOP TIME

⊗ Wired Input - Do not populate slot with detector card

INPUT FILE CONNECTION & PROGRAMMING CHART

LOOP NO.	LOOP TERMINAL	INPUT FILE POS.	PIN NO.	INPUT ASSIGNMENT NO.	DETECTOR NO.	NEMA PHASE	CALL	EXTEND	FULL TIME DELAY	STRETCH TIME	DELAY TIME
1A[1]	TB2-1,2	I1U	56	18	1	1	Y	Y			15✳
	-	J4U	48	10	26	6✳✳	Y	Y	Y		3
	-	I1U	56	18★	51	1	Y	Y			
1B	TB2-7,8	I2L	43	5	12	1	Y	Y			15
2A	TB2-5,6	I2U	39	1	2	2	Y	Y			
3A[2]	TB4-5,6	I5U	58	20	3	3	Y	Y			15✳
	-	J8U	50	12	28	8✳✳	Y	Y			3
	-	I5U	58	20★	53	3	Y	Y			
4A	TB4-9,10	I6U	41	3	4	4		Y		3.5	
4B	TB4-11,12	I6L	45	7	14	4	Y	Y			
5A[3]	TB3-1,2	J1U	55	17	5	5	Y	Y			15✳
	-	I4U	47	9	22	2✳✳	Y	Y	Y		3
	-	J1U	55	17★	55	5	Y	Y			
5B	TB3-7,8	J2L	44	6	16	5	Y	Y			15
6A	TB3-5,6	J2U	40	2	6	6	Y	Y			
7A[4]	TB5-5,6	J5U	57	19	7	7	Y	Y			15✳
	-	I8U	49	11	24	4✳✳	Y	Y			3
	-	J5U	57	19★	57	7	Y	Y			
8A	TB5-9,10	J6U	42	4	8	8		Y		3.5	
8B	TB5-11,12	J6L	46	8	18	8	Y	Y			

[1] Add jumper from I1-W to J4-W, on rear of input file.
[2] Add jumper from I5-W to J8-W, on rear of input file.
[3] Add jumper from J1-W to I4-W, on rear of input file.
[4] Add jumper from J5-W to I8-W, on rear of input file.

✳ Disable Delay during Alternate Phasing Operation.
✳✳ Disable Phase 2 & 6 and 4 & 8 Call for Loops 1A, 3A, 5A, and 7A during Alternate Phasing Operation.

★ See Input Page Assignment programming details on sheets 3, 4, 5, and 6.

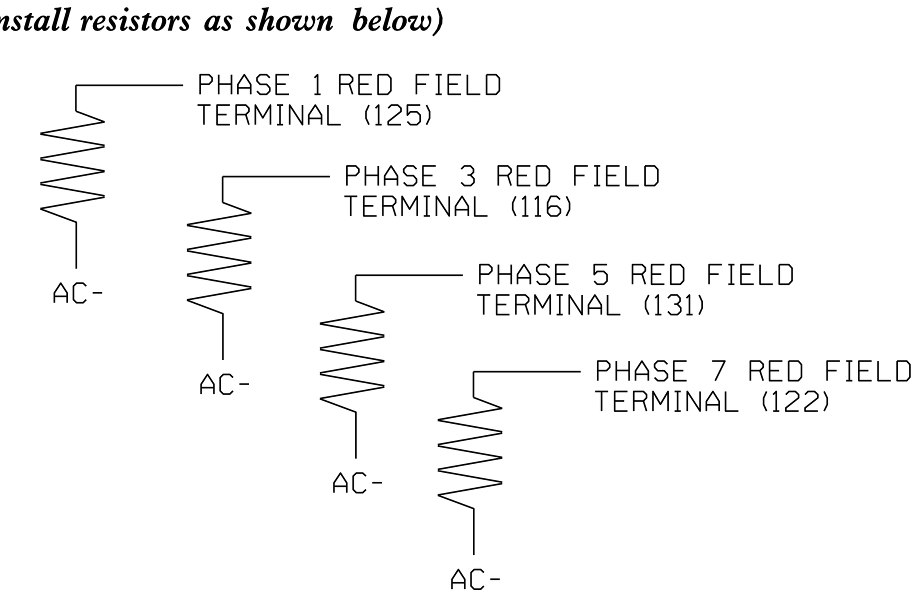
INPUT FILE POSITION LEGEND: J2L
FILE J
SLOT 2
LOWER

LOAD RESISTOR INSTALLATION DETAIL

(install resistors as shown below)

ACCEPTABLE VALUES

VALUE (ohms)	WATTAGE
1.5K - 1.9K	25W (min)
2.0K - 3.0K	10W (min)



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THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 06-1131
DESIGNED: Oct 2014
SEALED: 10/22/2014
REVISED:

Signal Upgrade - Final Signal - ELECTRICAL DETAIL SHEET 1 OF 7

ELECTRICAL AND PROGRAMMING DETAILS FOR:

Prepared for the Offices of:
Transportation Mobility and Safety Division
Signals Management Section
750 N.Greenfield Pkwy,Garner,NC 27529

SR 1102 (Gillis Hill Road)
at
SR 1112 (Stoney Point Road)

Division 6 | Cumberland County | Fayetteville

PLAN DATE: Oct 2014	REVIEWED BY: J.L. Lewis
PREPARED BY: D.J. Darity	VHB PROJECT NO.: 38286.02

REVISIONS	INIT.	DATE

SEAL
NORTH CAROLINA PROFESSIONAL SEAL 19713 ENGINEER DONALD J. DARITY

DocuSigned by: Don Darity
C80D150DC9834FE...
10/22/2014
DATE

SIG. INVENTORY NO. 06-1131

$$$$$SYSTIME$$$$$
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