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An ECONOLITE Group Company

Advanced System Controllers ASC/3 Maintenance Manual

P/N 100-0904-001 Rev. 03

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Controller	Warranty Period
ASC/3 Series Controller	2 years
Safetran ASC/3-RM Series Controller	2 years

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- Obtain a Return Authorization number from your sales representative.
- Pay all shipping charges to factory. Econolite will pay the return shipping charges.
- List on the packing sheet inside carton**:** the return Authorization No., Econolite's Sales Order No., your Purchase Order No., equipment Serial No., description of the problem with the equipment, and date of installation.

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Attn: Service Department
3360 E. La Palma Avenue
Anaheim, California 92806

OR

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Attn: Service Department
212 San Marco Avenue #B
St. Augustine, Florida 32084

(080424)

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1. INTRODUCTION

1.1. Purpose of this Document

This document is intended to provide theory of operation and maintenance information pertaining to the Advanced System Controller, Series 3 (ASC/3). The instructional data provided should enable qualified maintenance and repair personnel to appropriately service the ASC/3 controller. Instructions in this document should facilitate both the initial system unpacking and installation and also system maintenance and troubleshooting.

This manual contains the information needed to understand the hardware functions of the ASC/3 controller family. Information about the circuitry, general maintenance requirements, installation, and disassembly is included. Fault isolation charts are provided to help the technician isolate problems or to provide a good starting point for troubleshooting. Schematics and bills of material are included as well as several appendices to supplement the hardware descriptions.

1.2. Programming Manual

A separate *ASC/3 Programming Manual* (P/N 100-0903-006) is also available. That document provides basic programming and operational information pertaining to the ASC/3 series controllers. Instructional data provided in that manual is intended to enable qualified programming and operating personnel to easily enter appropriate software control parameters into an ASC/3 controller so as to properly configure the controller for both vehicular and pedestrian monitoring and control within a predefined traffic area.

1.3. Document Layout

This document is divided into five main chapters, followed by seven appendices.

1.3.1. Main Chapters

The main chapters of this manual are:

Chapter 1 – Introduction Describes the purpose and layout of this document.

Chapter 2 – Equipment Descriptions Provides brief physical and functional descriptions of each of the two controllers (ASC/3-1000 and ASC/3-2100) and also provides descriptions of general operational features.

Chapter 3 – Theory of Operation Contains detailed descriptions of circuit operations in the various ASC/3 modules with appropriate references to schematic and block diagrams also contained in this manual.

Chapter 4 – Maintenance Provides a collection of procedures and check lists that should be used as part of regular maintenance. Included are procedures for installation, disassembly, visual inspection, cleaning, battery check, and various adjustments. Test equipment and connector-cable assignment lists are also included. ASC/3 diagnostic tests, the primary method for hardware verification and fault isolation, are explained.

Chapter 5 – Troubleshooting Provides a Troubleshooting Chart that outlines a series of possible hardware, software, and programming problems along with their associated possible causes and suggested solutions.

1.3.2. Appendices

Appendix A – Schematics Contains schematic circuit diagrams for the ASC/3 controller modules.

Appendix B – Assembly Drawings Contains assembly drawings for all ASC/3 assemblies

Appendix C –Interface Connector Pin Lists Contains pin lists for all ASC/3 connectors A-D, SDLC, C1/C11, Terminal, and telemetry.

Appendix D – Bills Of Materials Contains Bills of Materials (BOMs) for parts used in ASC/3 controller assemblies.

Appendix E – System Interconnection Describes the standard system interconnection using Econolite telemetry interface boards and transient suppressors.

Appendix F – Guide to Lease-Line Installation Contains a guide to lease-line installation used in Econolite system communication.

Appendix G – Loopback Diagnostic Input/Output Tables Lists and identifies loopback diagnostic error codes.

Appendix H - TS1 Suitcase Diagnostic Testing Describes the TS1 Suitcase Test Screen HD-D and provides a table containing the ASC/3 TS2 I/O Address.

2. EQUIPMENT

2.1. ASC/3 Series General Features

The ASC/3 series of controllers includes two ShelfMount models, ASC/3-1000 and ASC/3-2100, and two RackMount models, ASC/3-RM 1000 (TS2-T1 only) and ASC/3-RM, C1, shown on the page that follows. All models have the same displays and keyboards on their front panels. The connectors, however, are very different:

- ASC/3-1000 and ASC/3-RM 1000 have a single fuse and a single “A” input/output connector; the only difference between these models is that the ShelfMount has the “A” connector and fuse on the front panel and the RackMount has them on the rear panel.
- ASC/3-2100 has two fuses and four input/output connectors, A, B, C, D.
- ASC/3-RM, C1, has Cal Trans standard 170/2070 C1/C11 connectors on the rear panel.

The ASC/3 controller designs use the latest microprocessor, display, and keyboard technology. Fewer components increase overall system reliability and allow an efficient use of space. Each controller has two main electronic modules that are accessible without the use of extender cards.

2.1.1. Equipment Enclosure Features

The ASC/3-1000 and ASC/3-2100 controllers can be enclosed in either a cast aluminum enclosure designed for shelf mounting within a large street-side cabinet or enclosed in a formed aluminum enclosure that is designed to be wall-hung within a smaller pole-mounted cabinet.

2.1.2. Central Processing Unit (CPU)

All of the ASC/3 controllers use the Motorola MPC862 Central Processing Unit and, as a result, all can run the same software applications and use the same database configuration. For these reasons, this maintenance manual is used for all controllers.

2.1.3. Power Supply

All the ASC/3 controllers have power supply assemblies that are easily accessible with only a screwdriver. Optional telemetry or RS-232 modules are available for system applications and are compatible with all controllers.

2.2. System Operating Characteristics

The ASC/3-1000, ASC/3-RM 1000, and ASC/3-2100 controllers function as semi-actuated or fully-actuated traffic controller units in accordance with the National Electrical Manufacturers Association (NEMA) Standards Publications TS1-1989 and TS2-1992.

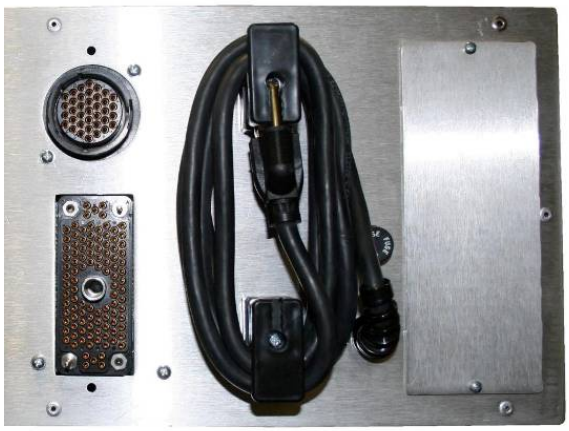
The ASC/3 series of controllers operate as 16 phase controllers with any combination of 16 vehicle phases, 16 pedestrian phases, and 16 timing overlaps along with eight concurrent groups and four timing rings. An application-specific configuration file may be specifically programmed to meet customer configuration requirements. In addition to the standard controller capabilities, the ASC/3 controllers provide outstanding software and hardware features that greatly simplify programming, operation, monitoring, and maintenance.

Programming is menu-driven and, in most cases, involves only option selections or numeric-value data entries. Numerous programming options give control flexibility and enhanced detector coordination that include non-interconnected coordination (NIC), time-of-day (TOD), preemption, and diagnostic capabilities. Real-time controller activity is monitored locally or remotely via dynamic status displays, which together show all controller dynamic parameters.

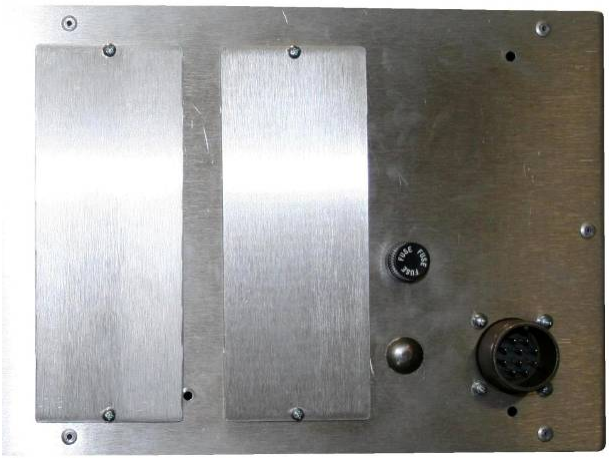
ASC/3-1000, ShelfMount

ASC/3-2100, ShelfMount

ASC/3-RM, RackMount, Front Panel



ASC/3-RM (C11), Rear View



ASC/3-RM 1000 (TS2-T1 only), Rear View

2.3. ASC/3 Series Controller

The ASC/3 series of controllers include the ASC/3-1000, ASC/3-RM 1000, ASC/3-2100, and the ASC/3-RM, C1. Each model provides the same control functions but uses different hardware input/output (I/O) configurations to interface with other components in a traffic control cabinet.

All models include three serial communication channels. The Port 1 channel is used to exchange data with a Malfunction Management Unit (MMU), retrieve vehicle detector data from detector racks and route I/O functions through Terminal and Facility Bus Interface Units (BIU). Port 2 is a terminal port with an RS-232 interface. Port 3A is another terminal port with and RS-232 interface. The optional Port 3B is a telemetry port using a frequency-shift-key (FSK) audio interface, available in a 9 pin FSK only interface or in a 25 pin FSK and telemetry I/O interface.

Also, there is a 10/100 MBPS Ethernet interface and a Datakey™ receptacle (these are optional in some units) for database storage and upload/download capabilities.

2.3.1. Input/Output Connectors

ASC/3-1000 and ASC/3-RM 1000

The single NEMA specified “A” connector on these controllers meets NEMA TS2 Type 1 requirements as referenced in NEMA TS2 3.3.4.

ASC/3-2100

This controller has NEMA specified “A”, “B”, “C” connectors and meets the NEMA TS2 Type 2 requirements referenced in NEMA TS2 3.3.5. In addition, an Econolite-specific “D” connector allows the model 2100 to replace any NEMA TS1, NEMA TS2, ASC-8000 or other controllers (with adapter cables), that include NEMA TS1, KMC-8000, and ASC-8000.

ASC/3-RM C1

This controller has Cal Trans standard 170/2070 C1/C11 connectors.

2.3.2. Port Interfaces

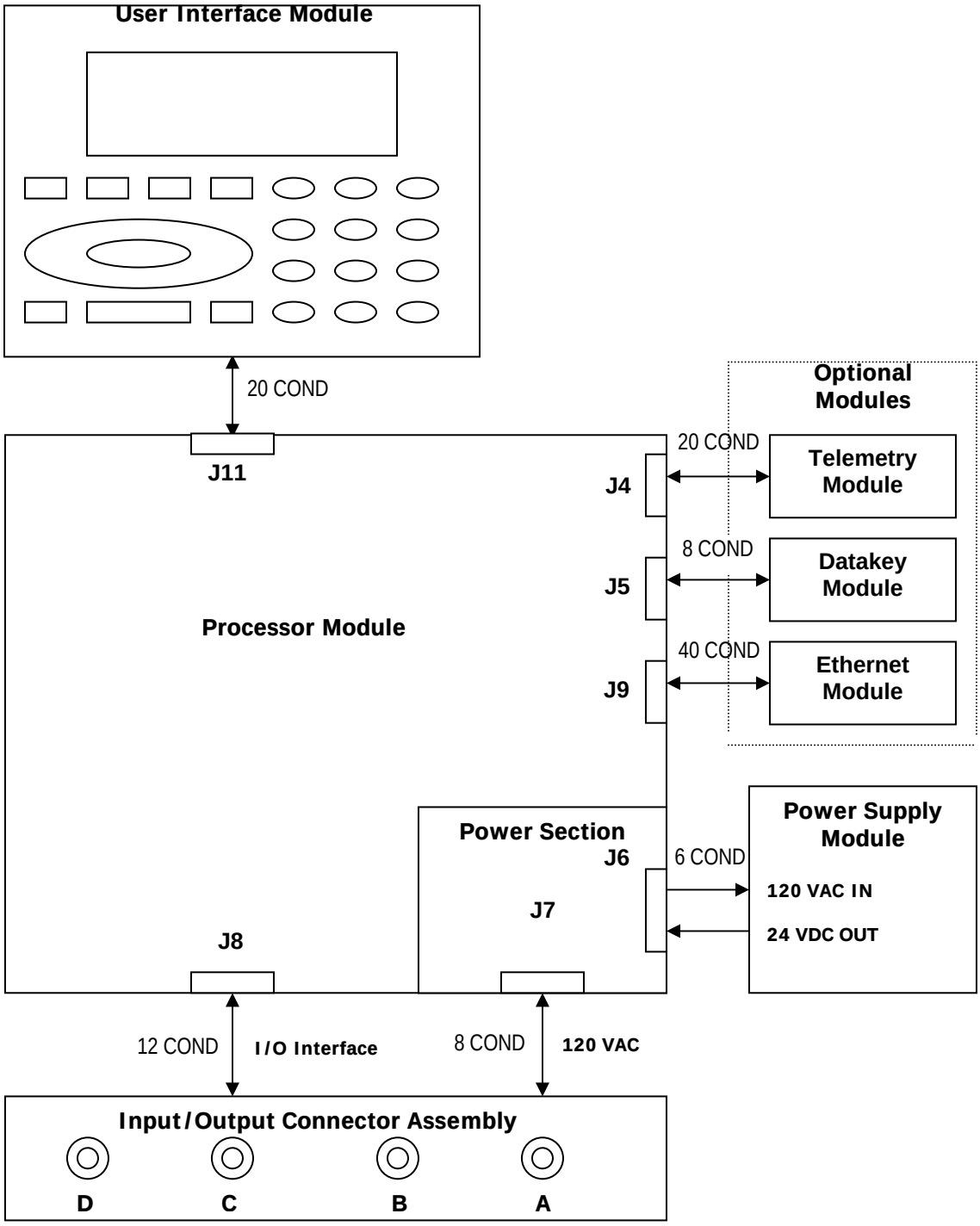
The Port interfaces for all ASC/3 controller models are:

- Port 1 NEMA TS2 3.3.1
- Port 2 NEMA TS2 3.3.2
- Port 3A NEMA 3.3.3 specified connector used for RS232 communication.
- Port 3B NEMA TS2 3.3.3 (optional plug-in module)

The ASC/3-1000, ASC/3-RM 1000 and ASC/3-2100 are similar, but the ASC/3-2100 provides a TS2 type 2 or legacy TS1 connector interface for cabinets that require these interfaces. The ASC/3-2100 can operate in NEMA TS1, TS2 type 1 and TS2 type 2 modes, whereas the ASC/3-1000 and ASC/3-RM 1000 can operate only in NEMA TS2 type 1 mode.

2.3.3. Memory and Electronic Modules

In all ASC/3 models of controllers, PROM memory has been replaced with Flash EPROM that allows faster and easier software upgrades. The ASC/3-1000 and ASC/3-RM 1000 have a single main electronic module that is accessible without the use of extender cards. The ASC/3-2100 adds a parallel I/O module, also accessible without the use of extender cards.



Note: ASC/3–2100 has connectors A, B, C, and D
ASC/3– 000 and ASC/3-RM 1000 have
only connector A

Typical ASC/3 System Block Diagram

2.4. Functional Description

The descriptions contained in the following paragraphs are intended to give you a basic understanding of functions performed by the various system modules that make up the ASC/3 system controllers. The circuit and signal descriptions that follow are best understood when studied together with the block diagrams and system schematics. The block diagrams are included in this chapter and schematics are located in Chapter 6.

2.4.1. Processor Module

The Processor-I/O module contains the microprocessor chip, memory chips and support circuitry required to operate and control all ASC/3 functions. This module also includes all I/O circuitry and controls the User Interface module keyboard and display operations. Slide through connector **J11** connects this module to the User Interface module.

The system buses include the address bus that identifies the device or memory location targeted for information exchange, the data bus that carries the information, and the control bus that synchronizes the data transfers. The communications buses include the Telemetry bus, SDLC bus, and Terminal bus which transfer serial data between the microprocessor and the universal asynchronous receiver transmitter (UART) chips and their associated interface chips.

The Processor-I/O module is connected to the power supply module via connectors **J6** and **J7**. The power supply provides +24VDC.

Auxiliary processor functions include a watchdog timer which checks for proper program operation, the voltage monitor which checks for power fail conditions, and the battery-backed clock circuit which keeps accurate time when power is removed from the unit. The system random access memory (RAM) is also powered by the battery backup circuit so that data integrity is maintained during power fail conditions.

Also included on the module is the AC line transient protection circuit and line referenced 120Hz interrupt generator.

The I/O interface section connects external inputs and output, with the microprocessor system address, data and serial communications buses. This allows the microprocessor to perform all input and output functions.

2.4.2. I/O Interface Modules

The I/O section of the Processor-I/O module consists of a bi-directional serial I/O chain, logic level translators, output latches, output drivers, serial communications interface circuits, and the telemetry module interface/expansion I/O connector J4.

External parallel inputs are applied through front panel connectors A, B, C, and D. The input voltage levels are translated to logic levels to be used by the system. The TRUE/FALSE (LOW/HIGH) states are then applied to an input serial chain. The processor reads the input status by scanning the serial input chain, thus transferring the input status into internal memory.

The processor uses output latches to control the external parallel signals. It addresses a specific output and latches that output status from the data bus by enabling the latch. The signal is then sent to external connectors A, B or C. In the event of a long power failure, the latches are cleared to prepare for an orderly controller re-start.

The Terminal bus signals interface with external equipment through Terminal connector J2 (PORT 2). It is used to communicate with printers, computer terminals or other controllers in the ASC family.

The SDLC bus signals interface with optional Bus Interface Units (BIUs) and/or a Malfunction Management Unit via SDLC connector J1 (PORT 1).

The Port 3A bus signals interface with external equipment through connector J3 (PORT 3A). It is used to communicate optional cabinet equipment, computer terminals or other controllers in the ASC family.

The Telemetry bus signals attach to slide through connector J4 and supply the signals required for an FSK channel, as well as an I/O and modem control interface. Once translated by the Modem module, the signals interface with external audio network signals via the telemetry modules Port 3B connector.

2.4.3. Voltage Monitor Control

Voltage monitor control is accomplished by monitoring the power supply output, battery voltages, and Processor signals. It is output to external equipment as VOLTAGE MONITOR.

2.4.4. Power Supply Module

The Power Supply module is a 40 watt, 24 volt off-line switching supply set for 120VAC operation. When configured as an ASC/3-2100 controller, input power is applied through the A-connector on the controller front panel and then routed, via the AC line transient protection circuit, to **J7** on the I/O module. A wire harness connects between **J7** and the processor module, which passes AC power to the supply module via **J6**. When used in the ASC/2S-1000 controller, input power is applied through the MS connector on the front panel and then routed via a cable assembly to the processor module, which passes AC power to the supply module as mentioned above. The +24VDC output from the supply is routed back to the Processor-I/O module via a wire harness connected to **J7.**

2.4.5. Telemetry Module

The optional Telemetry module operates as a transceiver providing communication between the ASC/3-1000, ASC/3-2100 and an ASC/2M-1000 or KMC-10000 master controller. The module is controlled by the Processor module and interfaces with the Telemetry bus via connector **J4**. Transmit, and receive signals are interfaced through Telemetry connector **3B** on the front panel.

Transceiver Operation

Communication between the local and master controllers is achieved over voice grade four-wire (two data channels) type 3002 leased telephone lines or customer owned cable. The telemetry data channel is made up of command (master to local) and readback (local to master) lines. Additional lease-line information is found in Appendix D. Each local transceiver is assigned a unique telemetry address used by the master to identify the transceiver. The address is assigned by either direct keyboard entry (refer to the ASC/3 Programming Manual). Devices connected to the local transceiver are identified by subaddresses assigned and used by the master.

The master generates command messages containing local telemetry address, message type, subaddress, data, and a horizontal parity word. Command messages are transmitted to the local transceiver in a predefined sequence. The sequence begins with a zero address command which simultaneously transmits to all local controllers, the system traffic program and four special functions. Local controllers do not respond to the zero address command. Subsequent messages request the status of the devices (listed above) connected to the local transceiver. The addressed local controller sends an appropriate response to the master on the readback line. Transmission of commands and readbacks occurs simultaneously. An error status is generated if a readback is not received by the master within a predefined period. For more information on master controller operation using telemetry, refer to the ASC/2M-1000 or KMC 10,000 Master Programming and Maintenance Manuals.

At the local transceiver, modulated command message signals are transformer coupled to the receiver where they are filtered and demodulated to a serial-bit pattern. The serial-bit pattern is

converted by an SCC receive channel on the microprocessor into a parallel pattern, four-word command message which is read by the microprocessor. If the message address corresponds to that of the local transceiver and if the message is valid, the microprocessor performs the operation specified by the message type. Where readbacks are required, the local transceiver generates a three-word readback message containing the requested data and horizontal parity word. The three data words from the microprocessor are converted to a serial bit pattern by a transmit channel on the UART. The serial bit pattern is then sent to the MODEM that provides frequency shift key (FSK) modulation for transmission. Valid data, transmit, and received carrier LEDs are ON or flash during normal data transmission.

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3. THEORY OF OPERATION

3.1. Introduction

This chapter contains detailed descriptions of the various ASC/3 modules. Each module is described in detail with references to schematics in the format [D - S,X,Y] where:

D is the schematic drawing number

S is the schematic sheet number within the above schematic drawing

X is the horizontal coordinate (numbers 1 through 6)

Y is the vertical coordinate (letters A through D)

Example: The **PI_TXC** signal on **U1 pin N18** [100-1013-601 – 2,3,D] defines and locates the signal being traced as follows:

PI_TXC is the signal being traced

U1 pin N18 is the circuit component and pin where the signal enters

100-1013-601 is the drawing number without the revision letter (see note below)

2 is the schematic drawing sheet number

3 is the horizontal coordinate

D is the vertical coordinate

NOTE: The schematic drawings included in your manual (Section 6) should be the appropriate revision level for the system equipment that you have received and installed. Therefore, the schematics you find there should appropriately reflect your system configuration.

Shortened Format: The drawing number is NOT always provided in this format. It is normally included at the beginning of each new module description or when the signal being traced enters a new drawing. Thereafter, only the sheet number and coordinates are given even if the signal is traced to several different sheets within a drawing. **Example: U18 pin6** [4,1,D]

Part Numbers: Part numbers (when given) are identified in parenthesis (###) immediately before references to schematic coordinates. **Example: U14** (74AHC245) [4,5,C] indicates the circuit component **U14** has part number 74AHC245 and can be found on sheet 4, coordinates 5 C, of the drawing previously referenced.

Use of Bold Type: As shown, signal names (**PI_TXC**), circuit component designators (**U14**) and pin numbers (**pin N18**) are all printed in **bold type**. Drawing numbers, part numbers, sheet numbers, horizontal and vertical coordinates are NOT printed in bold type.

Schematics and Block Diagrams: The schematic drawings are found in Chapter 6 of this manual. Also, a module block diagram is shown before the discussion of each module. These block diagrams illustrate general functional operation.

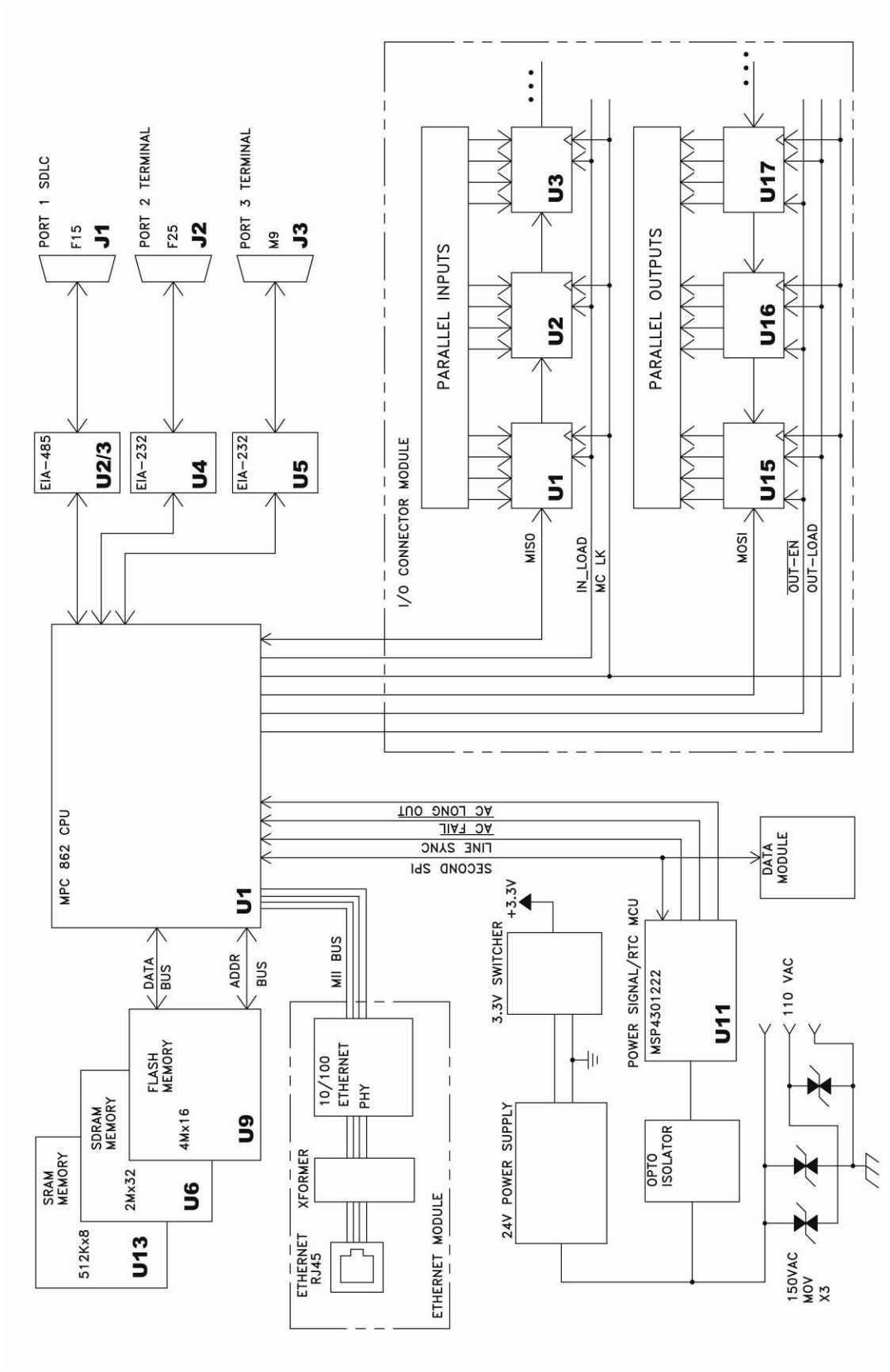


Figure 3-1 Processor Section Block Diagram

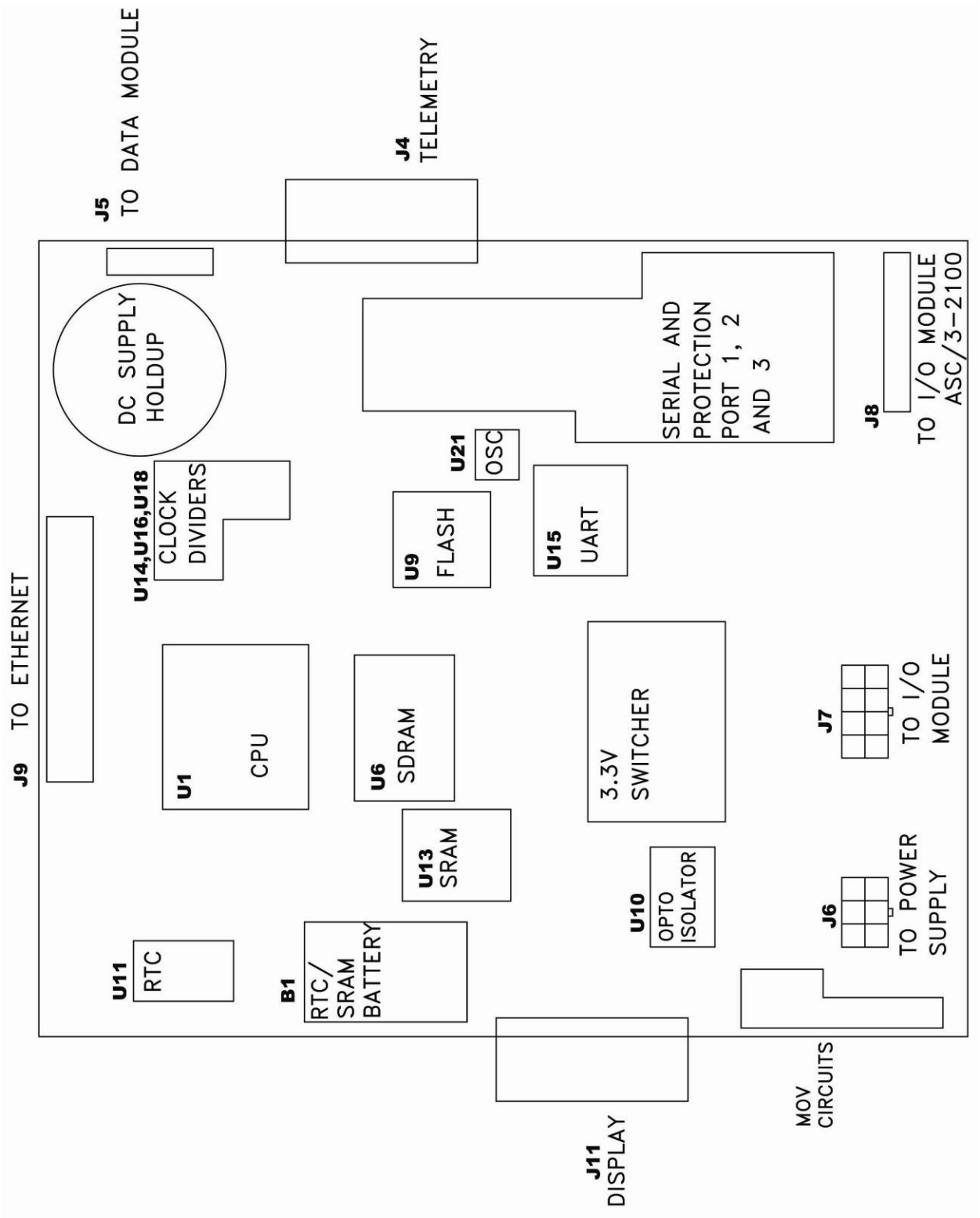


Figure 3-2 Processor Component Placement

3.2. Processor Module

See Appendix A for Processor Schematic.

3.2.1. Microprocessor

The ASC/3 series controllers use the Motorola MPC862 integrated multi-protocol processor **U1** [100-1013-601 – 2,2,B]. This is a Very Large Scale Integration (VLSI) Complementary Metal Oxide Semiconductor (CMOS) device that includes:

- A 32-bit power PC core processor,
- A system integration block, and
- A Reduced Instruction Set Computer (RISC) communications processor.

Features of the system integration block used by the ASC/3 include:

- The independent Direct Memory Access (DMA) controller,
- A multi-level interrupt controller,
- The dual port Random Access Memory (RAM) area,
- Three programmable timers,
- Eight programmable chip-select lines,
- Forty-six parallel I/O lines,
- An on-chip clock generator, and
- Several other "glue logic" functions.

The RISC Communications Processor (CP) provides the following functions:

- The main controller (RISC Processor),
- Four independent full-duplex Serial Communications Controllers (SCCs),
- Two independent full-duplex Serial Management Controllers (SMCs),
- Seven serial DMA channels for the six SCCs and SMCs,

A Synchronous Peripheral Communications “SPI” channel, and

An Ethernet Media Access Controller, which connects to a Media Independent Interface (MII).

The following paragraphs contain microprocessor signal descriptions. All relevant information about the microprocessor signals and their associated control circuits are discussed.

3.2.2. Clocks

The system clock synchronizes the internal operations of the microprocessor and all external devices on the system buses. Microprocessor timing is controlled by a 7.3728 MHz crystal oscillator **U21** [4,2,C] that forms a signal called **PPC_CLK** that is sent to **U1 pin N2** [2,5,B]. The 7.3728 MHz clock is also divided down in frequency to become an external UART clock and an SDLC transmit clock.

To create the external UART clock signal, the 7.3728 MHz clock is applied to **U17 pin 1** [4,2,D] where it is divided by 4 to become a 1.8432 MHz signal **ASYNC_CLK** which then connects to **U15 pin 18** [4,3,D] to become the external UART clock and is also sent to **U1 pin P17** [2,3,D].

To create the SDLC transmit clock, within **U17** the 7.3728 MHz clock is also divided by 8, then sent to **U18 pin 14** where it is further divided by 6 to result in the 153.6 KHz SDLC transmit clock signal named **P1_TXC** that is supplied to **U1 pin N18** [2,3,D], **U2 pin 5** [6,6,D], and **U3 pin 5** [6,6,C].

3.2.3. System Control Pins

The Power On Reset (**/PORESET)** signal at **U1 pin R2** [2, 5,B] is an input signal that, when asserted, causes a complete system reset. The **/PORESET** signal is generated [9,2,B] by **U20** via **U22E** and **Q4** in response to the core power voltage being out of tolerance. The reset logic additionally creates an **RST** signal **U22 pin 10** [9,1,A] and **/RST U20 pin 1** [9,2,A]. The **RST** signal is also a write protect mechanism for the battery backed SRAM on **U13 pin 10** [3,1,B].

3.2.4. System Buses

Data Bus (D0-D31)

Pins D0-D31 [2,4,D] form the data bus for the system. This 32-bit, bi-directional, three-state bus is the general-purpose path for exchanging data with memory and other system devices. It can transmit and accept data in byte, word, or double word widths. Power PC cores differ from conventional CPUs in that the data bus bit values are near opposites when compared with the bit memory bit-positions. For more information on this, please refer to the MPC862 programming reference.

8-bit accesses use a byte channel from D7-D0, where D0 is the most significant bit (MSB).

16-bit accesses use 2 word channels from D31-D16, and D15-D0, where D16 and D0 are the MSB's.

32-bit accesses use a double- word channel from D31-D0 where D0 is the MSB.

The data bus signals (D15 – D0) are also used to latch a power-on configuration word via U19 and U23 [9,6,C] which defines the boot device bus width and other important configuration parameters during system startup.

Address Bus (A0-A31)

Pins **A0-A31** [2,4,A] form a 24-bit address bus for the system. Each memory or I/O device that uses the address bus is allocated a specific chip select **/CS0 - /CS7** to select the attached device. The chip select is asserted based on an internally decoded memory map which sets up the address bus according to the internal access's mapping into the physical memory map. The address bus is used as a linear bus for all the asynchronous memory types (Flash ROM, Static RAM, UART and some I/O) but is multiplexed when used for synchronous memories (SDRAM).

Terminal Bus (Port 2)

This bus originates at the CPU on **U1 pins J17** (**P2_TX**), **G16** (**P2_RX**) both at [2,2,D], and at **R19** (**P2_DCD**), **M16** (**P2_CTS**) both at [2,1,C], and **E18** (**P2_RTS**) at [2,1,B]. These signals are all routed to **U4** [6,2,B/C/D], which acts as an EIA-232 level shifter. On the EIA-232 side of the level shifter, **TXD**, **RTS,** and **DTR** are outputs that go to **J2 pins 2, 4, and 20** [6,1,D]. **RXD**, **CTS**, **DSR** and **DCD** are all inputs that connect to **J2 pins 3, 5, 6, and 8** [6,1,D]. High voltage transient protection is provided by zener diodes **CR7** to **CR14** [6,1,B/C].

Terminal Bus (Port 3A)

This bus originates at the CPU on **U1 pins J16** (**P3A_TX**), **J18** (**P3A_RX**), **L19** (**P3A_RTS**) all at [2,2,D], and **K19** (**P3A_DCD**) at [2,1,B]. These signals are routed to **U5** [6,6,A], which acts as an EIA-232 level shifter. On the EIA-232 side of the level shifter, **TXD** and **RTS** are outputs that go to **J3 pins 2** and **7** [6,4,A]. **RXD**, and **DCD** are inputs that connect to **J3 pins 3** and **1** [6,4,B]. High voltage transient protection is provided by zener diodes **CR15** to **CR18** [6,4,A].

Telemetry Bus (Port 3B and Telemetry I/O)

The ASC/3 telemetry interface is achieved by providing a single serial UART channel via **U15** [4,3,C/D], as well as a serial control interface for the telemetry module provided by signals from **U1 pins K16** (**TLM_TX**) and **L16** (**TLM_RX**) both at [2,2,D]. These signals interface with the

optional telemetry module for purposes of modem configuration and a serial link for the telemetry I/O at **J4 pins 5** and **6** [8,6,D].

UART **U15** [4,3,C/D] provides a logic level interface to the telemetry modem module, which provides a physical layer conversion to the signals, and provides hardware flow control functionality to the modem. Some control signals are provided at **J4** [8,6.D] **pins 9** (**/TLM_INST**), **10** (**TLM_TYPO**), and **11** (**TLM_TYP1**).

These signals provide information to the CPU as to whether a telemetry module is attached and what type that module is. Additionally, sixteen 24VDC inputs and four open-collector outputs are provided.

SDLC Bus (Port 1)

This bus contains the serial data and clock signals that are routed to the SDLC Port (PORT1) EIA-485 interface chips **U2** and **U3** (ADM3491) [6,6,C/D]. Signals included in this bus are:

The receive data line at **U2 pin 2** (**P1_RX**), which inputs serial data to the CP on the processor,

The transmit data line at **U2 pin 5** (**P1_TX**) which outputs serial data from the CP and transmit,

The receive clock at **U3 pin 2** (**P1_RX**) needed to synchronize input communications over the SDLC channel, and

The transmit clock at **U3 pin 5** (**P1_TXC**) needed to synchronize communications over the SDLC channel.

SPI Input/Output Bus

The SPI (Serial Peripheral Interface) bus contains the serial data, handshake signals, and clock used for communications with the TS1/TS2, type 2 I/O connector interface. This bus interface forms a serial input and output shift register chain that allows up to 16 input bytes and 16 output bytes to be exchanged on this bus.

All of the following signals originate at **U1** [2,2,D]:

The SPI input bit at **U1 pin D19** (**SPI_MISO**),

The SPI output bit at **U1 pin E16** (**SPI_MOSI**), and

The SPI master clock signal at **U1 pin C19** (**SPI_CLK**).

The following signals are used to control data flow to the I/O Connector Module:

The SPI input load signal at **U1 pin U18** (**/IO_IN_LD**) which loads the serial input chain with input data prior to the serial shift,

The SPI output load signal at **U1 pin R17** (**IO_OUT_LD**) which loads the outputs after the serial shift, and

The SPI output enable signal at **U1 pin N16** (**/IO_OUT_EN**) which enables the outputs to be tri-stated or active.

Second SPI Bus

This bus forms a pseudo (or not a legitimate) hardware-driven SPI Bus. This bus provides a link of lower priority signals, such as the link to the Real Time Clock or to the Datakey™ serial data module. The Second SPI signals originate at **U1** [2,3,D] as follows:

U1 pin U19 (SSPI_MISO),

U1 pin T19 (SSPI_MOSI),

U1 pin R18 (SSPI_CLK).

Additionally, two chip selects are provided to select Real Time Clock or the Datakey module:

U1 pin P19 (/CS_MCU),

U1 pin M19 (/CS_DKEY).

3.2.5. External Interrupt Sources

An interrupt signal causes the processor to stop normal program execution and go to an address that is the beginning of an interrupt service routine. Executing the routine provides whatever action is necessary to service the device generating the interrupt.

/UART_INT

Connects to the CPU at **U1 pin U14** (**/IRQ1**) [2,5,C], which allows the UART to signal the CPU for service. This interrupt is the highest priority of the external interrupts.

/LINESINK

This connects to the CPU at **U1 pin W4** (**/IRQ5**) [2,5,C], which is a signal that requests service by the real-time clock interrupt routine. This AC line-referenced 60Hz square wave signal is generated by **U11**[7,4,C] in conjunction with optoisolator **U10** [7,3,A]. This routine controls timing of all controller software activity and provides real-time clock updates. This signal is the compliment to **LINESINK**, the pair effectively form a single dual edge triggered interrupt at 120Hz.

LINESINK

This connects to the CPU at **U1 pin V4** (**/IRQ6**) [2,5,C], which is a signal that requests service by the real-time clock interrupt routine. This AC line-referenced, 60Hz square wave signal is generated by **U11** [7,4,C] in conjunction with optoisolator **U10** [7,3,A]. This routine controls timing of all controller software activity and provides real-time clock updates. This signal is the compliment to /**LINESINK**, the pair effectively from a single dual edge triggered interrupt at 120Hz.

3.2.6. Internal Interrupt Sources

The MPC862 processor contains additional on-chip interrupt sources that can generate interrupts. The ASC/3 controller family uses the following interrupts: SCC1 through SCC4, SMC1, and SMC2, Port C10 bi-directional edge, the Fast Ethernet Controller (FEC), loss of PLL lock, and several high resolution timers.

Port 3B Interrupts

The Port 3B receive channel, which is used for the telemetry channel, is set up to generate an interrupt whenever a transmit or receive event has occurred or when a change of modem control line state has occurred (for hardware handshaking).

Port 2 Interrupts

The Port 2 receive channel, which is used for the terminal interface, generates an interrupt when an XON or XOFF character is recognized while the port is used for printing or when blocks of data of various predefined lengths are received from another device during the direct connect process.

Port 1 Interrupts

The Port 1 receive channel, which is used for the SDLC interface, generates an interrupt after a complete frame is received from a BIU or MMU.

Timer Interrupts

Timer 1 is used for the SDLC channel and generates interrupts that set the proper timing of the transmission of SDLC frames to the BIUs and MMU.

3.2.7. Memory

The ASC/3 controller has flash EPROM (Erasable Programmable Read Only Memory), SDRAM (Synchronous Dynamic Random Access Memory), SRAM (Static Random Access Memory), and an optional "Datakey™" data module. Each of these is separately described in the following paragraphs.

Flash EPROM Program Memory

The software program that controls processor operation is written into **U9** (E28F640J5A-120) [3,1,A]. This is a 120-nanosecond rewritable flash EPROM that provides 2 Megabytes of program address space configured as 1024K x 16 words, and 6 Megabytes of file system address space configured as 3072K x 16 words. Power On Reset (POR) boot code in **U9** starts the processor and allows the system and CPU to be configured to a point where the entire system image can be copied from the flash memory into SDRAM memory.

SDRAM

Program memory is provided by Synchronous Dynamic Random Access Memory (SRDRAM) **U6** or **U7+U8.** After the boot loader has loaded all the program memory into the SDRAM, the system restarts, this time booting from SDRAM, which since it is 32 bits wide, offers much faster execution as compared to flash operation. SDRAM memory offers additional benefits over the asynchronous flash memory in that the SDRAM memory is burstable.

SRAM

Runtime variable data is stored in Static Random Access Memory (SRAM) **U13** (55V040AFT) [3,1,A]. The ASC/3 provides 512K bytes of data memory. SRAM is powered by voltage **KAPWR** [9,1,D] so that data is not lost during power outages.

When the SRAM chip select signal **/CS2** is LOW and if the 3.3V power supply is good, the RAM reads or writes the data on the odd data bus **(D7-D0)** in the location specified by the address bus **(A31-A13)**. If the 3.3V power supply is not within its limits, writing to the SRAM device is inhibited by the **/RST** signal **U13 pin 10** [3,1,A].

3.2.8. Voltage Monitor Control

Both the Voltage Monitor "CVM" and the Fault Monitor "FM" outputs are under the control of MCU **U11** [7,4,C] (MSP430F1222). **U11** monitors all the local power supply inputs (**VCC_3V**, **VBAT**, **+24VI**, **+24VE**) and provides the voltage data to CPU **U1.** If the voltage of **VCC_3V** is not +3.3±.3v, or if +24VE is less than +16VDC, both /CVM_OUT and / FM_OUT (**U11 pins 17 and 18)** are driven HIGH, which in turn will turn on open collector drivers that interface the cabinet. In absence of a voltage failure, **U11** passes the digital values read from the **/CPU_CVM** and **/CPU_FM** inputs **U11 pins 21 and 24**.

3.2.9. Down Time Accumulator

The Down Time Accumulator (DTA) detects missing 120 Hz interrupts and times the length of power outages. The DTA consists of battery-backed MCU **U11**, which functions as a real time clock, as well as providing a filtered 60hz reference (**LINESYNC**) to the CPU **U1**.

****CAUTION****

Do not attempt to adjust the RTC crystal Oscillator capacitor **C17** in the field. This is a precision adjustment. See Maintenance Chapter 4 for proper adjustment procedure.

U11 also determines whether the length of a power failure is less than or greater than 0.75 seconds. This time was selected as the limit within NEMA range. If the power failure is less than 0.75 seconds the controller continues to operate. If the power failure is greater than 0.75 seconds the controller reverts to its start-up sequence. If power fails altogether, the processor writes its internal RTC time out to **U11** to keep accurate time until power is reapplied.

U11 uses a combination of **VCC_3V** and battery **B1** [9,2,D] voltage to operate. The processor communicates with **U11 pins 11, 12, 13,** and **14** [7,4,C] over the **Second SPI** bus. When power is reapplied, the processor reads the time from **U11** and updates its internal RTC time.

3.2.10. Local Voltage Regulators

Switching regulator **U12** (LM3485) [5,5,A] converts the incoming +24VDC into the +3.3VDC "**VCC_3V**" signal used throughout the module. Transient voltage suppressor **CR25** [5,6,A] protects the input from any transients greater than about +30VDC.

3.2.11. Back-Up Power Supply

The back-up power supply provides power to the SRAM and the battery-backed clock during a power failure. With power applied, the **VCC_3V** power supply provides power to the battery-backed real time clock **U11** [7,4,C] and the SRAM chip [3,2,B] as long as **VCC_3V** is greater than **VBAT**+0.1v.

Jumper **JP2** [9,2,D] disconnects the battery **B1** [9,2,C] during troubleshooting or periods of extended storage. **B1** is a rechargeable lithium battery and uses resistors **R36** and diode **CR29** as the charging circuit.

Battery voltage is monitored by MCU **U11**. When battery voltage drops below 2.2 VDC, MCU signals the CPU that the battery is not recharging properly and replacement is required.

3.3. User Interface Module

The User Interface module contains a Liquid Crystal Display (LCD) formatted as 16 lines of 40 characters, the display contrast control, the display backlight circuit, the display heater circuit, the keyboard matrix, and the system buzzer. The display contains its own control and drive electronics, and appears as two registers to the processor. The display is connected to the ASC/3 processor module via User Interface connector **J11** [100-1013-601 – 8,1D]. See Appendix A for User Interface Schematic.

Please note: The User Interface Module should be sent to Econolite for repair.

3.3.1. Display Interface

The ASC/3 application transfers one byte at a time from the display buffer via **D00-D07** to transceiver **U14** (74AHC245) [100-1013-601 – 4,5,C]. When both **/CS5** [8,1,B] and **/WE0** [8,1,C] are LOW, the data is transferred to the User Interface module data bus and routed to the

LCD modules data lines. The LCD module uses a combination of signals **/OE, /CS5, LCD_C_/D** on its inputs to transfer the data to its internal circuitry.

3.3.2. Keyboard

The User Interface module keyboard consists of a matrix of conductive rubber switches. The processor scans the matrix via **J11** by reading specific addresses. Writes to the register selected by **/CS4** bits 0 to 3 become the keypad row scan code via **U1** (74HCT374). The column data is read by reading the register selected by **/CS4 via U2** (74HCT244). The processor then decodes the four column status bytes to determine which key is pressed.

3.3.3. Backlight

The LCD module contains a matrix of yellow/green LEDs used to backlight the display. The backlight is enabled from the front panel.

The processor uses an output register to control the backlight control. **/CS4** is used along with **/WE0** to write the keypad control interface [8,1,C]. Writing a masked value of 0x40 will turn on the display backlight.

3.3.4. Buzzer

The processor uses an output register to control the buzzer control. **/CS4** is used along with **/WE0** to write the keypad control interface [8,1,C]. Writing a masked value of 0x20 will turn on the buzzer.

3.3.5. Heater

The processor uses an output register to control the heater control. **/CS4** is used along with **/WE0** to write the keypad control interface [8,1,C]. Writing a masked value of 0x80 will turn on the display heater.

3.4. Data Module

The Data Module [100-1007-601] is an option to the ASC/3 controller and, if equipped, its receptacle is mounted to the front panel sheet metal that allows the Data Module "Datakey™" to be inserted at any time. The Datakey™ provides a signal called **/DK_INST** on **J5 pin 8** [8,4,C], which notifies the processor when the Datakey™ is inserted or removed from its receptacle. The Datakey™ memory provides 512K bytes of serial, flash-based, non-volatile memory. The serial memory is interfaced by the Second Serial Peripheral Interface (SPI) at connector **J5** [8,4,C/D] **pins 3, 4, 5,** and **6** with signals (**/CS_DKEY**), (**SSPI_CLK**), (**SSPI_MOSI**), and (**SSPI_MISO**). [8,4,C].

3.5. Ethernet Module

The Optional Ethernet module [100-1006-601] is mounted to the front panel, and connects to **J9** [8,3,D] on the Main CPU board. The Ethernet Media Access Controller (MAC) provides a 10/100 base T interface, in half or full duplex and supports Auto-configuration of the link parameters. The electrical interface uses an industry standard MII (Media Independent Interface) to connect the MAC to the Physical Layer (PHY). The ASC/3 Ethernet module provides 2 diagnostic LED's, Link and RX activity. The PHY chip [2,4,C] is **U5**. The PHY interfaces the RJ-45 connector **J2** [3,1,C] via isolation transformer **T1** [3,3,C]**.** If the ASC/3 Ethernet is plugged onto an active Ethernet network, the rightmost **LED1** led should illuminate, which indicates a physical layer link between the ASC/3 PHY and the network device that it is connected to. During normal Ethernet traffic, you should also see the leftmost **LED1** LED light periodically, which indicates frame reception activity. The ASC/3 Ethernet module contains an I/O point (/ETH_INST) which when the Ethernet Module is installed, allows the Main CPU board

to detect its presence and initialize the internal network protocols. See Appendix A for Ethernet Schematic.

3.6. Models of ASC/3 Controllers

There are four basic models of ASC/3 Controllers, two Shelf-Mount models and two RackMount models, as shown in the table below.

The ASC/3-1000 and ASC/3-2100 both use the same Main CPU Module, but only the ASC/3-2100 uses TS2 type 2 Connector Board (Assembly Drawing 100-1008-501) which has four input/output connectors A through D and two fuses. The ASC3/-1000 and ASC/3-RM 1000 have a single connector A and a single fuse. The ASC/3-RM, C1 operates the same as a Cal Trans standard 2070-A.

For the theory of operation of two of the controllers, refer to the paragraph referenced in the last column of the table. Because the basic theory of operation is the same as for the ASC/3-2100, the theories of operation of the ASC/3-1000 and ASC/3-RM 1000 are not given.

ASC/3 Controller Model	Shelf Mount or Rack Mount	Single Connector A on the Front or Rear*	4 Connectors on the Front, A-D — 3 NEMA, 1 Econolite	2 Connectors on the Rear — C1/C11 Cal Trans standard 170/2070	Paragraph of the Theory of Operation
1000*	Shelf	Front			
RM 1000*	Rack	Rear			
2100	Shelf		X		3.7
RM, C1	Rack			X	3.8

* TS2-T1 only

3.7. ASC/3-2100 Parallel I/O Section (TS2 Type 2 Interface)

3.7.1. General

All processor access to the parallel I/O section is done via the SPI interface, which forms an input and output shift register chain. This bus contains the serial data, clock, and handshake signals which are used for communications with the TS1/TS2 type 2 I/O connector interface. This bus interface forms a serial input and output shift register chain, which allows up to 16 input bytes and 16 output bytes to be exchanged on this bus. The signals originate at the Processor Module [100-1013-601 – 2,2,D] component **U1 pins D19** (**SPI_MISO**) the SPI input bit, **E16** (**SPI_MOSI**) the SPI output bit, and **C19** (**SPI_CLK**) the master clock. The following signals are used to control the flow of data to the I/O Connector Module:

U1 pin U18 (**/IO_IN_LD**) that loads the serial input chain with input data before the serial shift.
U1 pin R17 (**IO_OUT_LD**) that loads the outputs after the serial shift.
U1 pin N16 (**/IO_OUT_EN**) that allows the outputs to be tri-stated, or active.

Power and Interface Circuitry (Schematic 100-1008-601, Sheets 1-7)

The I/O Connector Module is powered from **VCC_3V** and **+24VE**. The I/O circuitry however runs off 5VDC, so that power level is synthesized from the **VCC_3V** signal using a DC/DC charge pump converter **U30** [7,5,D]. The charge pump converter doubles the **VCC_3V** input voltage, then regulates that voltage down to 5VDC using **C4**, **C5** and is filtered using **C6**,**C7**, and **C8**. The external signal **CVM** is produced using inverter **Q1** [7,3,B] based on the **/CVM_OUT** signal from the Main CPU Module. Three volt to five volt interfacing is

accomplished using **U31** [7,4,B] to buffer the SPI interface output signals from the Main CPU Modules 3V logic levels to the I/O Connector Module 5V inputs.

3.7.2. Logic Level Translators

Each logic level translator (**R1 to R14**) consists of a three-resistor network (10K, 75K, and 18K) which converts the 24 V (FALSE), 0 V (TRUE) logic levels of control signals from external equipment to the HCMOS logic levels required by the input shift registers.

A 10K pull-up resistor biases the input to the FALSE state when the external control input is not connected. The voltage divider (75K and 18K) establishes the input level to the input register. An external input of 0 V to 8 V is detected as TRUE and an input of 16 V to 24 V is detected as FALSE (inputs are inverted internal to the processor). The combination of the 75K resistor, acting as a current limiter, and the internal protection circuit of the input register protects against transient input voltages exceeding 24 V.

3.7.3. Input Latches

Input serial shift register latches are used to interface data from the external connectors to the SPI bus. The processor controls the data transfer by latching the inputs and shifting the input bit stream into the SPI bus. The input registers are shown on sheets 3 and 4, showing **U1** to **U14. SOUT**, **pin 9** (74HC165) each higher order shift register feeds its **SOUT** signal into the previous stage's **SIN** input **pin 10** (74HC165). The input register is thus cascaded from **U14** to **U1** where the **U1 SOUT** pin connects to the **SPI MISO** signal at **J8 pin 4** [7,6,B]. The external inputs are all latched on the negative edge of the **SH_/LD_5V** signals on **pin 1** (74HC165).

3.7.4. Output Latches

Output serial shift register latches (**U15 to U29**) are used to interface data from the SPI bus to the external connectors. The processor controls the data transfer by enabling the latches and shifting the output bit stream through the output shift registers, and then latching the data from the registers to the physical outputs to be sent to external equipment. **MOSI_5V** is applied to **SIN U15 pin 3** (TPIC6B595) [5,6,D], and the **SOUT U15 pin 18** (TPIC6B595) [5,6,D] signal is cascaded into the next stages **SIN** pin, thus forming a cascaded serial output shift register. The **/OUT_EN_5V** (TPIC6B596) **pin 9** signals allow the outputs to be enabled when a LOW logic level is applied, or the outputs go tri-state when a HIGH logic level is applied. The **OUT_LD_5V** (TPIC6B595) **pin 12** signal, when strobed TRUE, allows the shift register output to be applied to the physical outputs. All output drivers are biased to the 24 V (FALSE) state, when not asserted, through a 10K pull-up resistor.

The TPIC6B595 output drivers are protected from transients on their output pins by Transient Voltage Suppressors (P6KE33A) that are installed on the CPU Main Module. These provide the output devices with a low impedance path to ground for voltages greater than 33VDC. This prevents damage to a driver by the reverse voltage generated when a relay coil connected to the output is de-energized or any other transient occurs.

3.7.5. I/O Scanning Process

At the beginning of an I/O sequence, the **/IO_IN_LD**, which normally dwells HIGH, is pulsed LOW for a brief period of time, which has the effect of latching the input shift registers chain (74HC165) by strobing the **/LD** input **pin 1**. The inputs are now stored in the serial input register chain.

Next, 15 bytes of output data is written out the SPI port, this data is the output bit stream destined for the output shift registers (TPIC6B595). While the outputs are being written, the inputs are being read on a bit by bit basis. Since the most significant output bit on the outputs is routed to the least significant output on the next shift register, the bits propagate through the entire shift register until the last bit of the last register is written.

After all the output bits have been written, the **IO_OUT_LD** control bit, which usually dwells LOW, is pulsed HIGH. The result is that the entire output bit stream previously written, is applied to the outputs simultaneously.

Also, since all the input bits were shifted in during the SPI output transfer, a buffer of 15 bytes is now inside the SPI peripheral, which can now be acted upon by the controller application.

3.8. ASC/3-RM, C1 Parallel I/O Section

3.8.1. General

All processor access to the parallel I/O section is done via the SPI interface, which forms an input and output shift register chain. This bus contains the serial data, clock, and handshake signals which are used for communications with the C1 and C11 Field I/O connector. This bus interface forms a serial input and output shift register chain, which allows up to 16 input bytes and 16 output bytes to be exchanged on this bus. The signals originate at the Processor Module [100-1013-601 [Zone 2, 2, D] component **U1 pins D19** (**SPI_MISO**) the SPI input bit, **E16** (**SPI_MOSI**) the SPI output bit, and **C19** (**SPI_CLK**) the master clock. The following signals are used to control the flow of data to the I/O Connector Module:

U1 pin U18 (**/IO_IN_LD**) that loads the serial input chain with input data before the serial shift.
U1 pin R17 (**IO_OUT_LD**) that loads the outputs after the serial shift.
U1 pin N16 (**/IO_OUT_EN**) that allows the outputs to be tri-stated, or active.

Parallel I/O section is constructed on a separate PCB that is mounted on the rear panel. This board contains the shift/latch open collector output registers, 12 V to TTL level input translators, shift/latch input registers, and the input/output Connectors, C1S and C11S.

3.8.2. Logic Level Translators

Since the I/O logic circuitry requires **5VDC** and the field inputs require **12VDC** on the 35151G101 and the processor logic levels on the 100-1013-601 are **3V**, there is an interface module 100-1119-501 (schematic 100-1119-601). This module translates the 3V signals to 5V via U2 A&B. The 5V signal is translated to 3V via R1 & R2. The 5V and 12V supplies for the 35151 are generated by U1 and U3 from the **+24VE**. Another function of the 100-1119-501 module is to generate a "code byte" (first byte on SPI MISO line) to tell the processor that the unit is an ASC/3 RM. This is accomplished by R4-R7 and U4.

3.8.3. I/O Scanning Process

SOUTBF connects to output shift register / latch / driver U2 (TPIC6B595) [Zone 1,6,C]. This signal then daisy chains through the remainder of the output devices. OUTSTRB, which is used to transfer the data from the shift registers to the output latches, connects to all TPIC6B595 in parallel. SHIFT connects to all the parallel I/O devices in parallel and carries the data from the input shift registers to the processor. The input shift chain starts at U2(74HC165) [Zone 2,6,C] and daisy chains through the remainder of the 74HC165s. INPSTRB, which is used to latch the input pin states into the shift registers, is connected to all 74HC165s in parallel.

Each input has a logic level translator made from three resistors such as RP3, RP2, RP1 [Zone 3,6,A-D]. This circuit provides a 10-kilohm pull-up to +12 VDC for the input device and converts the 0-12 VDC signal to CMOS compatible logic levels for use by the 74HC165 devices.
The TPIC6B595 output devices such as U2 [Zone 1,6,C] have open drain outputs.

3.9. SDLC (EIA-485) Interface

The SDLC interface circuit sends and receives its signals on the SDLC bus. All logic to EIA-485 signal level translation is provided by **U2** and **U3** (ADM3491) [6,6,D]. These contain one EIA-485 driver and one EIA-485 receiver each. After the signals are translated to EIA-485, they are routed to the outside world via connector **J1** (DA15S) [6,4,D]. The interface includes the following signals:

TXD+ and **TXD-** are the differential transmit data pair. The processor transmits this serial data signal as **P1_TX** from **U1** [2,3,D]. This signal is converted to a differential pair by **U2**. It is then output on connector **J1 pins 1** and **9**.

TXC+ and **TXC-** are the differential transmit clock pair. The processor transmits this serial data signal as **P1_TXC** from **U1** [2,3,D]. The signal is converted to a differential pair by **U3**. It is then output on connector **J1 pins 3** and **11**.

RXD+ and **RXD-** are the differential receive data pair. These signals appear on pins 5 and 13 of connector **J1**. After conversion by **U2**, the single ended logic level signal is routed to **U1** [2,3,D] on the processor as **P1_RX**.

RXC+ and **RXC-** are the differential receive clock pair. These signals appear on pins 7 and 15 of connector **J1**. After translation by **U3**, the single ended logic level signal is routed to **U1** [2,3,D] on the processor as **P1_RXC**.

/DSI_SDLC J1 pin 10 is provided to disable the SDLC communications for bench top testing. This is accomplished by grounding this signal to the local ground **J1 pins 2, 4, 6,** and **8.**

3.10. Terminal (EIA-232) Interface

The terminal interface circuit sends and receives its signals on the terminal bus. All logic level to EIA-232 signal level translation is provided by **U4** (ST3243) [6,2,D] which contains three EIA-232 drivers and five EIA-232 receivers. **U4** uses capacitors **C2, C3, C4,** and **C5** for its onboard positive and negative voltage generation circuits. Terminal signals are routed to the outside world via connector **J2** (DB25) [6,1,D]. The EIA-232 level signals are protected against over-voltage transients by transient voltage suppressors (MMBZ15VDLT1) [6,1,C]. The interface contains the following signals:

TXD is the transmit data signal. The processor outputs this serial signal from **U1** [2,3,D] as **P2_TX**. After translation, it appears on **J2 pin 2**.

RXD is the receive data signal. This serial input signal appears on **J2 pin 3**. It is translated and routed to **U1** [2,3,D] of the processor as **P2_RX**.

DCD is the Data Carrier Detect handshaking signal. This input signal appears on **J2 pin 8.** It is translated and routed to **U1** [2,3,D] of the processor as **/P2_DCD**.

CTS is the Clear To Send handshaking signal. This input signal appears on **J2 pin 5**. It is translated and routed to **U1** [2,3,D] of the processor as **/P2_CTS**.

RTS is the Request To Send handshaking signal. The processor outputs this serial signal from **U1** [2,3,D] as **/P2_RTS**. After translation, it appears on **J2 pin 4**.

DTR is the Data Terminal Ready handshaking signal. **U1** [2,3,D] outputs this serial **/P2_DTR**. After translation, it appears on **J2 pin 20**.

Signals **RTS, CTS, CD** and **DTR** are handled under program control and are implemented only as required. Communications with a printer use the **XON/XOFF** software handshake protocol.

3.11. Power Supply Module

3.11.1. AC Power Input

The AC line transient protection circuit consists of resistors **R76** and **R77**, and varistors **RV1, RV2,** and **RV3**. The circuit receives a three-wire, 120 VAC, 60 Hz input from the A connector on the I/O Connector Module (ASC/3-2100) or the power connector assembly (ASC/3-1000). The three inputs are AC line, AC neutral, and earth ground. AC line is over-current protected by fuse **F2**. AC line and AC neutral are then routed to current-limiting resistors **R76** and **R77,** respectively. Varistor **RV1, RV2,** and **RV3** provide both common and differential mode transient protection. This is accomplished by clamping transients occurring between AC line and AC neutral with varistor **RV2**. Transients occurring between AC line or AC neutral and earth ground are clamped by **RV1** and **RV3**, respectively. The output of the transient protection circuit is then applied to the power supply via connector **J6** [5,1,D]. Additional transient protection and noise filtering circuits are present on the power supply module.

3.11.2. Line Reference Circuits

Signal **AC_CROSS** is the 120 Hz line frequency reference used by the controller program as the input to the real time clock. Signal **AC_CROSS** is generated by full-wave rectifier **CR23** [20,3,C] that rectifies the 120 VAC 60 Hz line voltage to produce a 120 Hz signal. That 120 Hz signal is presented to the dual optoisolator **U10** (MCT6.S). Zener diode **CR24** (1N4763A) prevents output of the **AC_PF_DET** signal when the line voltage is below 82 VAC. Both signals are processed by MCU **U11** (MSP4301222) [7,4,C], which generates **LINESYNC** (used as an interrupt), **/AC_FAIL**, and **/AC_LONG_OUT** signals that are read by the CPU **U1** to detect AC power fail events. MCU **U11 pin 19** outputs a filtered, line locked, 60Hz **LINESYNC** signal that is used for timekeeping when the controller is AC powered.

3.11.3. Processor-I/O DC Input Circuit

The +24VDC enters the Processor-I/O module on connector **J6**. Diode **CR22** (MBRS340T3) [5,1,C] provides reverse polarity protection. **CR19, CR20,** and **CR21** provide current steering for the proper charging and discharging of the hold-up capacitor **C76**. **R31** limits in-rush current while charging **C76**. **+24VE** is the primary onboard +24VDC voltage source for I/O devices. **+24VI** supplies +24VDC to the +3.3VDC voltage regulator in the processor section. The **+24VEXT** external output is applied to connector pin A-B. This output is rated at 500 mA and provides sufficient current for most traffic applications. The 24 VDC has been fused with a 3/4 Amp SLO-BLO fuse, **F1**, to allow the controller to supply sufficient current for a controller test fixture using LED displays (20 mA per LED). This higher current capability should only be used during testing. Note that the 24 VDC load in the traffic control cabinet should never exceed 500 mA. Inductor **L2** [5,1,B] filters out noise induced on the logic ground (**FGND**) when it is run outside the controller.

3.12. FSK Telemetry Module

3.12.1. Overview

This Telemetry module [100-1032-50x] is offered in 2 models, the 9-pin Frequency Shift Keying (FSK) module, and the 25-pin FSK module with Telemetry I/O. Both models feature an internal digital signal processor (DSP), which is used as a general processor, and for its signal processing capabilities for FSK modulation and demodulation (Modem). This Telemetry module supports industry standard 1200 and 9600 BPS baud rates, and can operate as a full or half duplex interface. This Telemetry module forms a physical layer interface between the host device (the ASC/3), and an external network of similar modem devices.

The TMS320VC5502 DSP **U1** is the core of the FSK system, and processes digital representations of analog signals, and interfaces an external codec device TLV320AIC23B **U2**,

which forms a ADC/DAC combo for reading and writing analog signals to the FSK physical layer. The codec is interfaced by the DSP high speed synchronous interface (McBsp). Clock and framing signals are provided by the codec device, and the DSP in turn receives/produces the data stream at 96,000 samples per second.

This Telemetry module can run in a full or half duplex mode. Switch **SW1** is provided to physically link the transmit and receive transformers. If half duplex, 2-wire mode is selected, the single wire pair is connected to the TXD± terminals on the front panel connector. Additionally, **SW1** provides a signal named **FDUX/#HDUX** that notifies the DSP of the state of **SW1**, thus detecting the physical connection so that half duplex transmitter echo can be rejected.

3.12.2. FSK Receiver Input

The FSK waveform is applied to transformer **L1** via **J1** or **J3**, and is coupled differentially to a virtual ground, biased at half the analog rail voltage. **D4** clamps any transient voltages applied to the FSK receiver, thus protecting the module. **U17** and associated circuitry forms an anti-aliasing filter with a roll off designed to prevent high frequency tones from beating against the sample rate of the codec which could create artificial sub-tones that may interfere with the internal frequency detectors. The output of the input filter is capacitivly coupled to the codec left and right inputs, where the capacitor is driving against **R21** which holds the AC value centered to 1/2 the codec analog supply voltage of +3.3V.

3.12.3. Codec (ADC/DAC)

The codec samples the input and digitizes the values using a delta sigma, analog to digital conversion process which gets sent to the DSP via the McBsp interface. Signal **CLKRX1** originates at the codec and is the synchronous clock for the interface. Signal **FSX1** and **FSR1** (transmit **X** and receive **R** frame sync signals) are used by the DSP to determine the start of the 32 bits of data (16 bits left and 16 bits right) of both the ADC and DAC data channels.

DX1 and **RX1** are the data input and output signals for the interface; **DX1** is the DAC output bit stream from the DSP, and **RX1** is the ADC output bit stream from the codec. In normal operation, you should see a continuous clock on **CLKRX**, and frame sync signals on both **FSX1** and **FSR1** at 96khz. **DX1** and **RX1** bit streams are dependant on the specific signals coming and going to the Telemetry module, but you should not expect a continuous unchanging value on either signal.

The codec provides an analog output from its DAC which is filtered by **U16** and its associated components. This filter also provides additional gain in order to scale from the codec 3.3v supply to the analog sections 5V supply rail. The filter roll off is designed such that the modulated frequencies of interest are preserved but that the 96kHz sample rate is rejected in order to keep that noise from the transmit transformer. The transmitter is turned on and off by the DSP with node **XMIT_ON**, which has the ability to tri-state the output filter when the transmitter is off "**XMIT_ON** is LOW". The output impedance of the transmitting transformer (**L2**) is set to 600 ohms by **R25**. Since the output impedance is 600 ohms, connection of a resistive 600 ohm load to the transmitter pair will result in a drop in amplitude of 3db.

3.12.4. Power Supplies

The Telemetry module has four separate power supplies for the various functions and circuitry. **VCC3V** (+3.3VDC) is provided by **U5**. **U5** serves as a current inrush limiter, and hot-swap controller. After the initial inrush of current at power on, the input and output terminals of this IC are connected by an internal MOSFET switch. **VCC5V** (+5.0VDC) is generated by **U1** using **VCC3V** as its input. **U1** is a charge pump switching supply that multiplies its input voltage by 1.5 or 2.0 times then regulates that voltage to 5.0 VDC using an internal regulator. **C4** and **C5** are the "flying" capacitors in the charge pump, and they in turn charge **C6**, **C7** and **C8** at the higher voltage. **VCC2V5** (+2.5VDC) is generated by **U4** using **VCC5V**, and forms a virtual

ground for the **VCC5V** supply. This effectively forms a ±2.5V analog power supply for the analog section of the Telemetry module, and provides a low impedance virtual ground for the transmitter and receiver. **VCORE** (+1.25VDC) is generated by **U6** using **VCC3V**, and provides the internal DSP core with its operating voltage. This regulator is a "low drop out" type regulator and can get relatively hot during operation, so apply caution when working nearby this component.

3.12.5. Telemetry I/O

On Telemetry modules that include the 25-pin connector, additional inputs and outputs (Telemetry I/O) are provided for use by the host device. **U12** and **U13**, with pull-up networks **R10** and **R11**, form the 16 input points. **U12** and **U13** perform level conversion between the inputs and the DSP 3.3V I/O system. **U14** forms the four Telemetry outputs, and the resistor network **R16** pulls the open collector outputs to the 24V level.

3.12.6. Telemetry Processor

The Telemetry module DSP core section is the workhorse of the system. The DSP (**U8**) is essentially a microcontroller unit with internal DSP instruction capabilities. The DSP loads its startup instruction code from the serial flash PROM **U7** after power on reset. Power supply monitor **U9** monitors the **VCC3V** supply and provides the reset signal to the DSP. The DSP clock (and codec clock) is derived from oscillator **U10**. Upon power up, the DSP executes an internal boot loader application from internal ROM. This boot loader in turn reads the program information from the **U8**, and loads it into the internal program RAM. After the boot loader detects the end of the binary record in **U8**, it begins to execute the loaded application from its internal RAM. The DSP interfaces the host controller (the ASC/3) via general purpose I/O interfaces, and by an internal UART interface (**HOST_TX/ HOST_RX**). **HOST_TX** and **HOST_RX** form an asynchronous control interface (115.2kbps) between the host and the Telemetry module processor. The purpose of this interface is to allow the host device to configure the functionality of the Telemetry module to gain access to device status, and to provide an interface for the Telemetry I/O, if so equipped.

3.12.7. Detailed FSK operation

This Telemetry module continuously monitors the receiver FSK signal, and demodulates its output to the **MODEM_TX** signal which is received by the host. This signal is the asynchronous bit reproduction of the FSK audio signal which was modulated by the modem connected to the Telemetry module receiver pair.

The host starts communication by asserting the **MODEM_RTS** input. Once the Telemetry module **MODEM_RTS** input is asserted, the module waits for a short delay period and then asserts the **MODEM_CTS** signal, which tells the host to begin transmitting on the **MODEM_RX** line. The host then de-asserts the **MODEM_RTS** signal, and the telemetry module times a carrier turn off interval and then de-asserts its **MODEM_CTS** signal to the host. The whole process is performed automatically in response to desired transmissions by the host device. While the transmitter is enabled (more or less when the **MODEM_CTS** signal is asserted), the DSP samples the **MODEM_RX** input value, converts it to an audio FSK bit stream and sends it to the codec DAC. The analog signal gets amplified and transmitted to the outside world via L1.

3.13. FSK and EIA-232 Telemetry Module

3.13.1. Overview

This Telemetry module [100-1084-50x] is offered in 2 models, the 9-pin module, and the 25-pin module with Telemetry I/O. Both models are capable of FSK or EIA-232 communications and feature an internal Digital Signal Processor (DSP), which is used as a general processor, and for its signal processing capabilities for FSK modulation and demodulation (Modem). For FSK,

the telemetry module supports industry-standard 1200 and 9600 BPS baud rates, and can operate as a full or half duplex interface. For EIA-232, standard baud rates between 1200 and 115.2kbps are supported. The Telemetry module forms a physical layer interface between the host device (the ASC/3), and an external network of similar modem devices.

3.13.2. Digital Signal Processor

The TMS320VC5502 DSP **U1** is the core of the FSK system, and processes digital representations of analog signals, and interfaces an external codec device TLV320AIC23B **U2**, which forms a ADC/DAC combo for reading and writing analog signals to the FSK physical layer. The codec is interfaced by the DSP high speed synchronous interface (McBsp). Clock and framing signals are provided by the codec device, and the DSP in turn receives/produces the data stream at 96,000 samples per second.

This Telemetry module can run in full or half duplex mode. Use Jumper **JP1** on the Main Circuit Board to select full or half duplex mode—for jumper location and positions, refer to the illustrations on the subsequent two pages. Jumper **JP1** physically links the transmit and receive transformers. If half duplex, 2-wire mode is selected, the single wire pair is connected to the TXD± terminals on the front panel connector. Additionally, **JP1** provides a signal named **FDUX/#HDUX** that notifies the DSP of the state of **JP1**, thus detecting the physical connection so that half duplex transmitter echo can be rejected.

3.13.3. Select FSK or EIA-232

The modules' EIA-232 interface uses a single chip, charge-pump-based transceiver that converts the EIA-232 signal level to +3.3VDC signals. There are a series of jumpers to configure the module to operate in FSK or EIA-232 mode. To configure the jumpers for a 9-pin Telemetry Module, refer to Figure 3-3 on the page that follows.

To configure a 25-pin Telemetry Module, use the same illustration of the circuit boards and, for the jumper positions, refer to the table on Page 3-19.

NOTE: On the circuit boards, the "EIA-232" jumper positions are labeled "RS232".

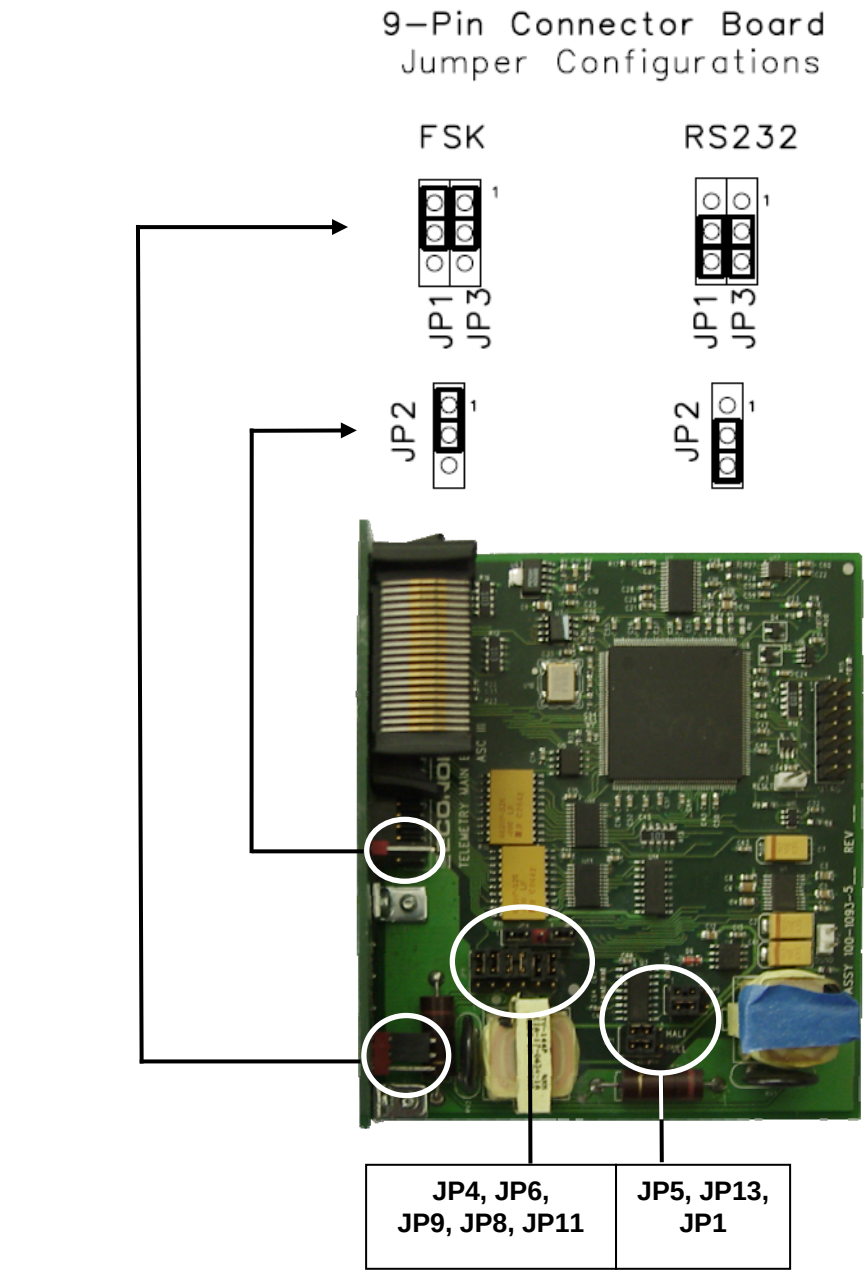
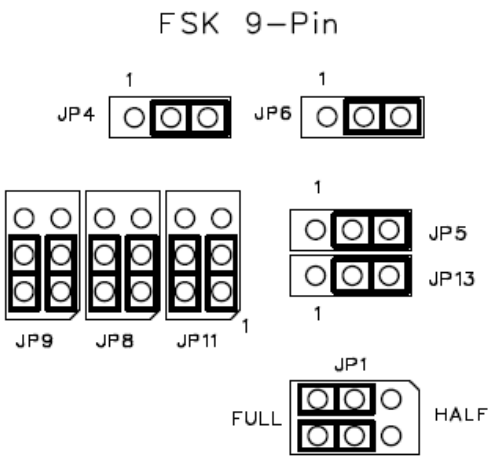
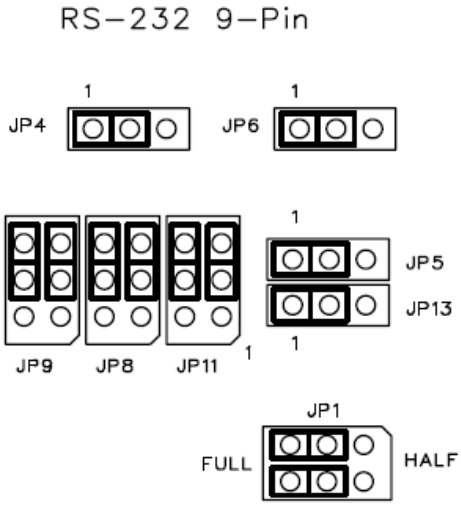


Figure 3-3

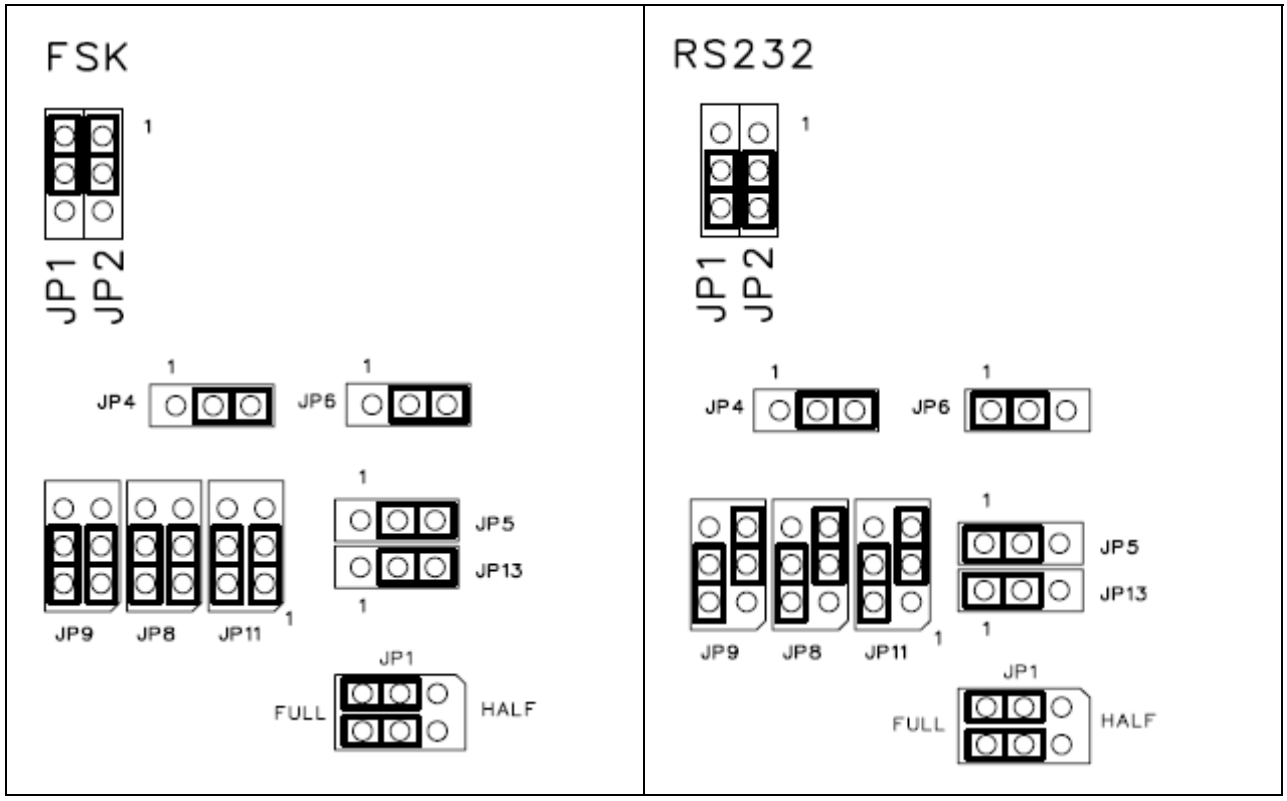
FSK or EIA-232
Telemetry Module
100-1084-50X
9-Pin

Front Panel Not Shown
for Clarity





Jumper Positions for the FSK & EIA-232 Telemetry Module, 100-1084-50X, 25-Pin
(For the locations of the jumpers, refer to the illustration on the previous page.)



NOTE: There are two **JP1** jumpers. The **JP1** on the Main Circuit Board is to configure Full or Half Duplex. The **JP1** on the Daughter Board is to configure FSK or EIA-232.

3.13.4. FSK Receiver Input

The FSK waveform is applied to transformer **L1** via **J1** or **J3**, and is coupled differentially to a virtual ground, biased at half the analog rail voltage. **D4** clamps any transient voltages applied to the FSK receiver, thus protecting the module. **U17** and associated circuitry forms an anti-aliasing filter with a roll off designed to prevent high frequency tones from beating against the sample rate of the codec which could create artificial sub-tones that may interfere with the internal frequency detectors. The output of the input filter is capacitively-coupled to the codec left and right inputs, where the capacitor is driving against **R21** which holds the AC value centered to 1/2 the codec analog supply voltage of +3.3V.

3.13.5. Codec (ADC/DAC)

The codec samples the input and digitizes the values using a delta sigma analog to digital conversion process which gets sent to the DSP via the McBsp interface. Signal **CLKRX1** originates at the codec and is the synchronous clock for the interface. Signal **FSX1** and **FSR1** (transmit **X** and receive **R** frame sync signals) are used by the DSP to determine the start of the 32 bits of data (16 bits left and 16 bits right) of both the ADC and DAC data channels.

DX1 and **RX1** are the data input and output signals for the interface; **DX1** is the DAC output bit stream from the DSP, and **RX1** is the ADC output bit stream from the codec. In normal operation, you should see a continuous clock on **CLKRX**, and frame sync signals on both **FSX1** and **FSR1** at 96 khz. **DX1** and **RX1** bit streams are dependant on the specific signals coming

and going to the Telemetry module, but you should not expect a continuous unchanging value on either signal.

The codec provides an analog output from its DAC which is filtered by **U16** and its associated components. This filter also provides additional gain in order to scale from the codec 3.3v supply to the analog sections 5V supply rail. The filter roll off is designed such that the modulated frequencies of interest are preserved but that the 96kHz sample rate is rejected in order to keep that noise from the transmit transformer. The transmitter is turned on and off by the DSP with node **XMIT_ON**, which has the ability to tri-state the output filter when the transmitter is off "**XMIT_ON** is LOW". The output impedance of the transmitting transformer (**L2**) is set to 600 ohms by **R25**. Since the output impedance is 600 ohms, connection of a resistive 600 ohm load to the transmitter pair will result in a drop in amplitude of 3db.

3.13.6. Power Supplies

The Telemetry module has four separate power supplies for the various functions and circuitry. **VCC3V** (+3.3VDC) is provided by **U5**. **U5** serves as a current inrush limiter, and hot-swap controller. After the initial inrush of current at power on, the input and output terminals of this IC are connected by an internal MOSFET switch. **VCC5V** (+5.0VDC) is generated by **U1** using **VCC3V** as its input. **U1** is a charge pump switching supply that multiplies its input voltage by 1.5 or 2.0 times then regulates that voltage to 5.0VDC using an internal regulator. **C4** and **C5** are the "flying" capacitors in the charge pump, and they in turn charge **C6**, **C7** and **C8** at the higher voltage. **VCC2V5** (+2.5VDC) is generated by **U4** using **VCC5V**, and forms a virtual ground for the **VCC5V** supply. This effectively forms a ±2.5V analog power supply for the analog section of the Telemetry module, and provides a low impedance virtual ground for the transmitter and receiver. **VCORE** (+1.25VDC) is generated by **U6** using **VCC3V**, and provides the internal DSP core with its operating voltage. This regulator is a "low drop out" type regulator and can get relatively hot during operation, so apply caution when working nearby this component.

3.13.7. Telemetry I/O

On Telemetry modules that include the 25-pin connector, additional inputs and outputs (Telemetry I/O) are provided for use by the host device. **U12** and **U13**, with pull-up networks **R10** and **R11**, form the 16 input points. **U12** and **U13** perform level conversion between the inputs and the DSP 3.3V I/O system. **U14** forms the four Telemetry outputs, and the resistor network **R16** pulls the open collector outputs to the 24V level.

3.13.8. Telemetry Processor

The Telemetry module DSP core section is the workhorse of the system. The DSP (**U8**) is essentially a microcontroller unit with internal DSP instruction capabilities. The DSP loads its startup instruction code from the serial flash PROM **U7** after power on reset. Power supply monitor **U9** monitors the VCC3V supply and provides the reset signal to the DSP. The DSP clock (codec clock also) is derived from oscillator **U10**. Upon power up, the DSP executes an internal boot loader application from internal ROM. This boot loader in turn reads the program information from the **U8**, and loads it into the internal program RAM. After the boot loader detects the end of the binary record in **U8**, it begins to execute the loaded application from its internal RAM. The DSP interfaces the host controller (the ASC/3) via general purpose I/O interfaces, and by an internal UART interface (**HOST_TX/ HOST_RX**). **HOST_TX** and **HOST_RX** form an asynchronous control interface (115.2kbps) between the host and the Telemetry module processor. The purpose of this interface is to allow the host device to configure the functionality of the Telemetry module to gain access to device status, and to provide an interface for the Telemetry I/O, if so equipped.

3.13.9. Detailed FSK operation

The Telemetry module continuously monitors the receiver FSK signal, and demodulates its output to the **MODEM_TX** signal which is received by the host. This signal is the asynchronous bit reproduction of the FSK audio signal which was modulated by the modem connected to the Telemetry module receiver pair.

The host starts communication by asserting the **MODEM_RTS** input. Once the Telemetry module **MODEM_RTS** input is asserted, the module waits for a short delay period and then asserts the **MODEM_CTS** signal, which tells the host to begin transmitting on the **MODEM_RX** line. The host then de-asserts the **MODEM_RTS** signal, and the telemetry module times a carrier turn off interval and then de-asserts its **MODEM_CTS** signal to the host. The whole process is performed automatically in response to desired transmissions by the host device. While the transmitter is enabled (more or less when the **MODEM_CTS** signal is asserted), the DSP samples the **MODEM_RX** input value, converts it to an audio FSK bit stream and sends it to the codec DAC. The analog signal gets amplified and transmitted to the outside world via L1.

3.13.10. External Power Supply

This module includes a UA78M12 linear regulator on the connector board to convert the internal +24VDC to +12VDC at 100mA maximum for use with external fiber optic modems. This feature is jumper-selectable and can only be used in the EIA-232 mode. The +12VDC source is provided on **pin 13** of the 25-pin connector module. On the 9-pin module, the +12VDC source is provided on **pin 7**.

4. MAINTENANCE

4.1. Introduction

Several procedures, guides, and lists are provided for general maintenance of the ASC/3 series. This section contains unpacking and installation procedures useful for the first ASC/3 installation and for later reference. A disassembly procedure instructs on removing each module and major components.

Basic procedures include printed circuit board cleaning, voltage checking, and down time accumulator crystal adjustment. A list of test equipment recommended for maintenance is also included. The circuit components used in the ASC/3 require care in handling, installing, storing, and operating both un-mounted and mounted on printed circuit boards

Modules and their components should only be handled at a static-free workstation. Personnel and equipment MUST be properly grounded. Please refer to the Motorola CMOS LOGIC data book or any other MOS manufacturer's procedures for more information.

4.2. Unpacking

The ASC/3 controller is packed in a specially designed protective shipping carton. All necessary precautions have been taken to ensure that equipment arrives intact and in proper working order. However, you should follow these steps when unpacking the controller to verify that there is no shipping damage.

Carefully inspect the shipping container for damage before opening. If the container is damaged, unpack the controller unit in the presence of the carrier.

Save the packing materials as they have been specially designed to protect the controller during shipment. The special packing materials must be used should it be necessary to ship the controller again.

Carefully inspect the controller for damage. Check for broken wires, broken connectors, loose components, bent panels, and dents or scratches on the enclosure.

If you discover any physical damage, notify the carrier immediately.

4.3. Installation

Install ASC/3-1000 and ASC/3-2100 controllers in a location where the front panel is easily accessible. Leave adequate room around the controllers to allow easy servicing and component removal. Ensure that the vents on the back of the controllers are not blocked.

Before applying AC power, perform the following checks:.

1. Open the front panel and verify that all modules are properly secured and all connectors are in place. Check to make sure that all ASC/3 socket-mounted components are properly seated.
2. If the controller is an ASC/3 equipped with a battery, the lithium-cell battery (B1) is mounted in the upper left of the Processor Module beside connector J11. Activate this battery by moving the JUMPER on JP-2 to the left-to-center (1-2) ON position. This jumper is located above J11.
3. If the intersection cabinet is equipped with an MMU or CMU that latches Fault Monitor (FM) or Controller Voltage Monitor (CVM), the monitor power-on flash time must be set (using the jumpers on the monitor program card) to a value of 9 seconds or greater.

The controller is now ready for installation. Cable connector part numbers are shown on the next page. Refer to Appendix B for pin lists for all interface connectors and to Appendix C for system interconnection instructions.

4.3.1. Cable Connectors and Part Numbers

CONNECTOR	CABLE CONNECTOR	ECONOLITE PART NUMBER
A	MS-3116-22-55S	44143P1
B	MS-3116-22-55P	44143P2
C	MS-3116-24-61P	44143P3
D	AMP #205842-1	31163P2
CRIMP SOCKET	AMP #66504-3	31663P4
SDLC (Port 1)	CANNON DAU-15P	54665P4
TERMINAL (Port 2)	CANNON DBU-25P	54665P7
TELEMETRY (Port 3A/B)	CANNON DEU-9S	54647P9
TELEMETRY (Optional)	CANNON DBU-25S	54647P6
POWER (Type 1)	MS-3106-18-1S	44181P1
C1 (ASC/2RM only)	AMP 201692-3	37134P2
I/O (ASC/2RM)	Cannon DCU-37P	54665P5

4.3.2. Environmental Operation Specifications

The ASC/3 controller meets or exceeds the NEMA environmental standards for traffic control equipment summarized below.

(NEMA TS2-1992 SECTION 2)

CATEGORY	REQUIREMENT
Ambient Temperature	Operating Range: -35°C to +74°C Storage Range: -45°C to +85°C
Humidity	Relative humidity is not to exceed 95% over the temperature range of +4.4°C to +43.3°C
Vibration	The controller will maintain its programmed functions and physical integrity when subjected to a vibration of up to 0.5g at 5 to 30 cycles per second, applied in each of the three mutually perpendicular planes.
Shock	The controller will not suffer either permanent mechanical deformation or any damage that renders the unit inoperable when subjected to a shock of 10g applied in each of the three mutually perpendicular planes.

4.4. Storage

Should it be necessary to store the ASC/3-1000 or ASC/3-2100 controller with power removed, **THE BATTERY SHOULD BE REMOVED OR DISCONNECTED BY SETTING THE BATTERY JUMPER (JP-2) TO THE CENTER-TO-RIGHT (2-3) OFF POSITION.** The battery is located at the upper left of the Processor module, beside connector J-11.

4.5. Test Equipment

The following is a list of suggested test equipment to be used for fault isolation, basic check-out, and general maintenance procedures.

1. 100MHz, digital, dual-trace oscilloscope. Used for observing signals and checking of time relationships of two waveforms where necessary.
2. Digital Multimeter (DMM). Used for continuity testing, diode and transistor checks, and general voltage measurements. The DMM should meet the following specifications:

PARAMETER	RANGE	ACCURACY	INPUT IMPEDANCE
DC Volts	200mV-1000V	±0.25% of Input	
AC Volts	200mV-750V	Humidity	10 MΩ, Capacitance < 100 pF
Resistance (Ohms)	200Ω-20MΩ		

3. Frequency Counter. Used for Down Time Accumulator (DTA) crystal adjustment. Note that the DTA crystal adjustment is a high precision adjustment. Therefore, an accurate frequency counter is required.

4.6. Disassembly

Below is a disassembly description for each module.

**** CAUTION ****

When disassembling the controller always disconnect input power (applied through front panel connector A) before attempting to disassemble any part of the controller.

4.6.1. Processor Module

The Processor-I/O module is attached to the enclosure by two 1/4-turn fasteners. To remove the module:

1. Disconnect the interface cable to the front panel.
2. Turn the fasteners 1/4 turn to the left.
3. Hold onto the assembly by the connector plate and pull the module out from the bottom until it slides out of the card guide on the inside top of the enclosure.
4. Pull the module out far enough to disconnect the two power supply harnesses attached to the rear of the module.

4.6.2. Power Supply

The power supply is mounted on standoffs above the processor module on the front panel. The supply is held in place by four screws and washers. To remove the Power Supply module:

1. Remove the two wire harnesses from the power supply module.
2. Remove the four screws and washers.
3. Remove the supply from the assembly.

4.7. Cleaning and Inspection

General controller maintenance includes regular cleaning and inspection of the controller printed circuit boards (PCBs), electronic components, connectors, cables, and plastic and metal parts of the enclosure.

Use the following cleaning and inspection procedure to prolong equipment life and to minimize the risk of failure.

4.7.1. Cleaning

**** CAUTION ****

Do not apply any cleaning solvents to keyboards, front panel, display, or any other plastic parts.

1. Disconnect the power source (front panel connector A) before attempting to clean any of the controller components.
2. When boards are repaired, clean flux residue from solder connections with an environmentally safe flux remover. Free air dry.
3. Clean keys and front panels with a soft, lint free, damp cloth. Free air dry. Do not allow excessive amounts of water to collect around or enter keyboard and display areas.
4. Clean PCBs with a non-abrasive, moisture and residue free aerosol duster.

4.7.2. Inspection

The following inspection guide is provided as a quick reference when inspecting the controller and its components.

Visual Inspection Guide

ITEM	DEFECT
Capacitors, general	Burned spots, damaged leads.
Capacitors, ceramic or tantalum	Broken or cracked bodies.
Capacitors, electrolytic	Ruptured bodies, leaking electrolyte.
Connectors	Broken, loose, bent, corroded, or missing pins; cracked insulation; or incorrect polarization.
Equipment, general	Dented or bent. Dust, dirt, lint, grease, oil; excess resin, spattered solder, metal chips, filings, or other foreign matter in equipment. Worn spots or deep scratches on surfaces, marred protective finish exposing bare metal, evidence of arcing, loosening screw thread assemblies.
Hardware, general	Incorrect screw length. Missing screws, nuts, bolts, rivets, lock washers and screws, nuts, nut plates, or bolts with stripped threads.
Integrated circuits	Broken or cracked bodies, corrosion, shorted contacts.
Markings, decals, and reference designators	Missing, incorrect, illegible, or obliterated.

ITEM	DEFECT
Printed circuit boards	Broken, cracked, or burned parts; broken or missing rivets; broken circuitry; chipped contacts; copper showing on contacts; copper showing on circuitry; cracks, holes, or burns in cards; defective soldering joints; cracks; flat surfaces; bubbles or holes; lifted pads; broken or missing eyelets.
Resistors	Discolored body, loose connections.
Solder connections	No solder, insufficient solder, excess solder, cold or crystallized joints.
Transformers	Melted insulation compound, frayed insulation
Terminal strips and boards	Cracked, burned, or damaged terminal pins
Wiring	Cut, burned, or abraded insulation exposing bare conductor, abrupt V bends which weaken conductor; points of abrasion not insulated; pinched or damaged wires; broken or loose lacing; loose clamps.

4.8. Lithium Battery Safety Information

The lithium-cell battery (B1) mounted in the upper left side of the Processor-I/O module supplies power to the CMOS RAM and the Battery Backed Clock during a power failure. This battery is rechargeable and should not require replacement during the life of the controller. However, lithium cells or batteries are very high-energy power sources and therefore must be handled with care. If a battery ever does require replacement, **please observe the following precautions:**

Do not short battery terminals. If a lithium battery or cell is short-circuited or overheats, immediately disconnect it from the load by removing the jumper from JP2 (on the upper-left or the I/O Processor module near the battery and connector J10).

Do not open, puncture, or crush batteries. Cells and batteries contain hazardous sulfur dioxide and flammable materials.

Dispose of properly. Do not incinerate. Do not compact for disposal. Cells and batteries can be disposed of in sanitary landfills. However, discharged lithium cells and batteries may contain significant amounts of unused energy and should be packed carefully and electrically isolated before disposal.

4.9. Telemetry Tests

Required Test Equipment:

- Test Loopback Cable 33279G6.
- Oscilloscope
- Master controller.

1. Set SW1 to the full duplex position (FULL).
2. Turn off controller power. Install module in controller. Reapply power.
3. Attach a 600 ohm load loopback cable (P/N 33279G6) to telemetry connector.
4. From the boot menu, execute the Port 3B loopback test (BOOT-7-6).
5. Verify that the test passes.
6. Set oscilloscope to 5 Volts/Division and 0.1mSec/Division.
7. Connect the scope to the TX and RX pairs of an existing FSK network, where a master has been configured for normal operation. Be certain that there are 600 ohm terminators on each set of pairs. Be sure that only the single controller is connected to the network.
8. Restart the controller, this time running the controller application (Asc3App).
9. Configure the Port 3B parameters as follows:

   Protocol = ECPIP

   Port = ENABLED

   BAUD = 1200

   FRAMING = 801

   Transmit response time = 0.1

   RTS to CTS time = 2.0

   RTS turn off time = 3.0

   Address = (any address the master is configured to use)

10. Install module in test controller. Attach telemetry Master cable to Port 3.
11. Set proper telemetry channel.
12. If controller is attached to an ASC/2M, set telemetry response delay on controller to 8800. (Set ASC/2M "TELEMETRY WINDOW to 80.) If controller is attached to a KMC 10,000, set telemetry response delay to 10,000.
13. Verify that the controller is responding to the master's commands by checking that the VALID LED is ON, and the TX led is blinking with a constant cadence.
14. Verify that controller communicates with master by looking at the master (MM-3-6) screen which shows the number of responses to transmissions.
15. With the scope, verify that the controller's transmit pair is transmitting a packet envelope (burst of FSK audio patterns, then quiet the output until the next burst).
16. Verify that the amplitude on the controller's transmitter pair is 2.29vpp ±.4vpp (0dbm)
17. Remove test equipment.

4.10. Hardware Diagnostic Tests

4.10.1. General Information

The ASC/3 Controller hardware diagnostic tests are part of the ASC/3 Boot software package. To access the Boot Menu, proceed as follows:

While powering up the ASC/3 controller, simultaneously press the “1” and the “CLEAR” keys. The Boot Menu Screen (shown below left) should appear.

Press the “7” key and the Hardware Diagnostic Menu (Screen HD, shown below right) should appear.

BOOT MENU SCREEN

```
02/14/2005      BOOT MENU        00:00:00

 1. DOWNLOAD FILES    6. SET WORKING DIR

 2. UPLOAD OPTIONS    7. RUN H/W DIAGS

 3. FILE SYSTEM       8. CLOCK/CALENDAR

 4. SETUP NETWORK     9. SHOW BOOT CFG

 5. SELECT APP        0. RESTART


     PRESS KEYS 1..9, OR 0 TO SELECT
```

SCREEN HD

```
          HARDWARE DIAGNOSTIC MENU

 1.  DISPLAY           8.  TELEMETRY I/O
 2.  KEYPAD            9.  S-RAM
 3.  PORT1             0.  ETHERNET
 4.  PORT2             A.  RTC/OTHER
 5.  PORT3A            B.  DATA MODULE
 6.  PORT3B            C.  AUTO-LOOP
 7.  TS2 "ABCD" I/O    D.  TS1 SUITCASE


                 PRESS
            0..9 TO SELECT 0-9
        SPEC FUNC 1-4 TO SELECT A-D
```

4.10.2. Selecting Hardware Diagnostic Menu Options

The Hardware Diagnostic Menu (shown above) displays the 14 diagnostic test options. Select option 1 through 0 by pressing the appropriate numeric key. To select options A, B, C, or D, press the SPEC FUNC key followed by a numeric key 1, 2, 3, or 4 for A, B, C, or D, respectively.

4.10.3. LCD Display Diagnostic Test

To select the Display diagnostic test while viewing the Hardware Diagnostic Menu screen, press the “1” key.

The test begins automatically and first performs tests of the Backlight On, Backlight Off, and Beeper functions. You can physically observe if these three tests are successfully performed. The display screen Backlight first turns on, then off, and then the beeper sounds.

Next, an LCD Display Screen test is performed in which a pattern is displayed on the LCD display screen that uses all available on-screen characters.

Finally, a Pixel test is automatically performed to check that all pixels in the LCD display screen are functioning properly.

If all tests are successfully performed, the screen shown below appears. If any test fails, an appropriate message appears to explain the nature of the failure.

SCREEN HD-1

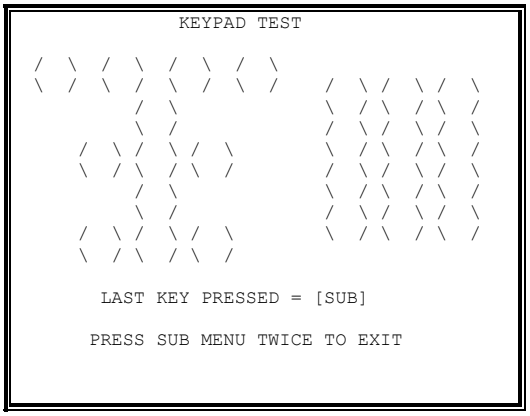
```
          LCD DISPLAY TEST



             *************
             *TEST PASSED*
             *************
        PRESS ANY KEY TO RETURN
```

4.10.4. Keypad Diagnostic Test

To select the Keypad diagnostic test while viewing the Hardware Diagnostic Menu screen, press the “2” key. The screen HD-2 shown at the right should appear. This screen shows a pattern of parenthesis marks ( ) arranged in a pattern similar to the pattern of the function and numeric keypads on the controller front panel.

The Keypad diagnostic test is an interactive test in which you actively press each key on the functional keypad to test to see if the signal from that key is being interpreted correctly. As you press each key, the space between the appropriate pair of parentheses should darken and the “LAST KEY PRESSED = “message should indicate which key was just pressed. When all keys have been pressed, all sets of parenthesis pairs should be darkened.

SCREEN HD-2

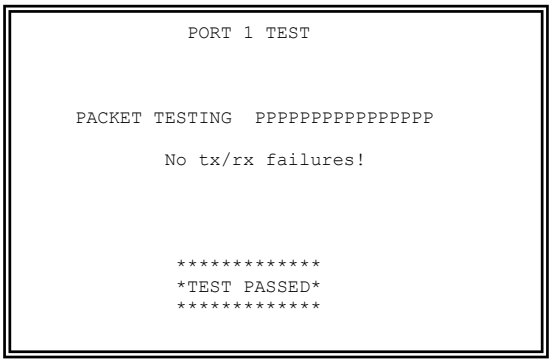


4.10.5. Port 1 Diagnostic Test

To successfully perform the Port 1 diagnostic test, a Port 1 loopback cable (P/N-33279G7) must be installed on the Port 1 SDLC front panel connector.

When the test is run, it automatically creates 16 output packets that are received as inputs through the loopback cable, and any detected faults are reported as response or frame failures on the display screen. If there are no transmit or receive (TX/RX) failures, Screen HD-3 (shown at the right) will appear to indicate the controller has passed the test.

SCREEN HD-3

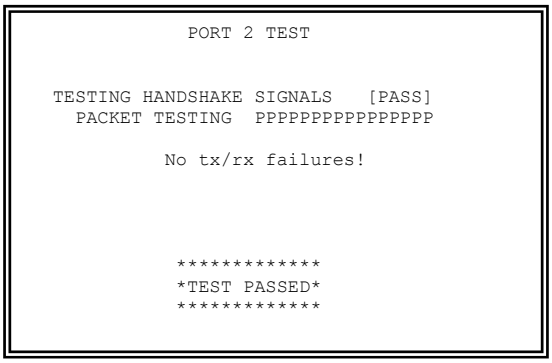


4.10.6. Port 2 Diagnostic Test

To successfully perform the Port 2 diagnostic test, a Port 2 loopback cable (P/N-33279G8) must be installed on the Port 2 TERMINAL front panel connector.

When the test is run, it automatically creates 16 output “handshake signal” packets that are received as inputs through the loopback cable ‘and any detected faults are reported as response or frame failures on the display screen. If there are no transmit or receive (TX/RX) failures, Screen HD-4 (shown at the right) will appear to indicate the controller has passed the test.

SCREEN HD-4



4.10.7. Port 3A Diagnostic Test

To successfully perform the Port 3A diagnostic test, a Port 3A loopback cable (P/N-33279G9) must be installed on the Port 3A TELEMETRY front panel connector.

When the test is run, it automatically sends 16 output packets that are received through the loopback cable and any detected faults are reported as non-response "N," or frame failures "F" on the display screen. If there are no transmit or receive (TX/RX) failures, "P" will be printed on the display for each packet sent. Screen HD-5 (shown at the right) will appear to indicate the controller has passed the test.

SCREEN HD-5

```
                PORT 3A TEST


TESTING HANDSHAKE SIGNALS    [PASS]
  PACKET TESTING  PPPPPPPPPPPPPPPP

            No tx/rx failures!



             *************
             *TEST PASSED*
             *************

         PRESS ANY KEY TO RETURN
```

4.10.8. Port 3B Diagnostic Test

To successfully perform the Port 3B diagnostic test, a Port 3B loopback cable (P/N-33279G?) must be installed on the TELEMETRY front panel connector slot.

When this test is run, it automatically tests both the data and control signals and also reports on both the P3B and P3C packet transmit/receive (TX/RX) failures. If there are no detected failures, Screen HD-6 (shown at the right) will appear to indicate the controller has passed the test.

SCREEN HD-6

```
      TELEMETRY INTERFACE LOOPBACK

TESTING CTRL SIGS            [PASS]
TESTING HANDSHAKE SIGNALS    [PASS]

PACKET TESTING P3B  PPPPPPPPPPPPPPPP
            No tx/rx failures!

PACKET TESTING P3C  PPPPPPPPPPPPPPPP
            No tx/rx failures!

             *************
             *TEST PASSED*
             *************
```

4.10.9. TS2 "ABCD" I/O Diagnostic Test

To successfully perform the TS2 "ABCD" I/O diagnostic test, appropriate loopback cables must be installed on connectors A, B, C, and D of the I/O module as follows:

Connector	Cable Part Number
A	33279G1
B	33279G2
C	33279G3
D	33279G4

When the test is run, it automatically tests 118 input/output connections through the loopback cables and any detected faults are reported (by number) on a failure display screen (typical shown at right top). Detected faults are displayed in two separate formats, each consisting of 4 characters as follows:

NOTE: A table in Appendix H of this manual supplies the Signal Description Type (Input or Output), I/O Address, and Cable Connector Pin Designation for each address tested.

Fault codes that begin with the letter "I" show that the input address (in hex format) is stuck in either high "H" or low "L." For example, I27L indicates input 27 is stuck LOW and I4cH indicates that input 4c is stuck HIGH.

NOTE: Only inputs are tested in this manner, so a fault code starting with 0 is a zero, not the letter O.

Fault codes that DO NOT start with the letter I, are a 4-character hexadecimal code where the first two digits are the OUTPUT address and the second two are the INPUT address. For example, as shown on "Screen HD-7 Failed" below, the number 3827 shows that output 38hex failed with its expected connection to input 27hex.

If there are no defective I/O point failures, "Screen HD-7 Passed" (also shown below) appears and indicates the controller has passed the test.

SCREEN HD-7 - FAILED

```
          TS2 TYPE 2 LOOPBACK
     Testing output 118
   Input  94 has failed with Output 118

3827 3830 3831 3832 391f 3a2b 3b25 3c33
3d41 3e42 3f44 4034 4133 4234 433a 443d
4446 4539 4638 4735 4843 4934 4a3d 4a46
4b40 4c3f 4d45 4e47 4f3c 5036 5133 5242
533e 543e 5537 5636 5735 5845 5938 5a44
5b65 5c62 5d61 5d67 5e68 5f63 6064 6166
624c 635d 64 ************* 4d 684b 694a
6a60 6b55 6c *TEST FAILED* 54 7053 7152
7256 7358 74 ************* 5a 765c 765e
2c2c 2c2e 2d1c 2e21 2f1e 2f2d 3048 313b
         PRESS ANY KEY TO RETURN
```

SCREEN HD-7 - PASSED

```
          TS2 TYPE 2 LOOPBACK

       Testing output 118




             *************
             *TEST PASSED*
             *************
        PRESS ANY KEY TO RETURN
```

4.10.10. Telemetry I/O Diagnostic Test

To successfully perform the Telemetry I/O diagnostic test, a Telemetry loopback cable (P/N-33279G?) must be installed on the 25 pin Telemetry module connector and a Telemetry module must be connected.

SCREEN HD-8

```
          TELEMETRY I/O LOOPBACK




             *************
             *NO HARDWARE*
             *************

          PRESS ANY KEY TO RETURN
```

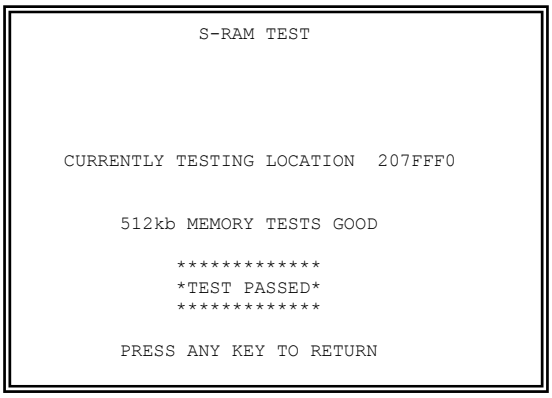
4.10.11. S-RAM Diagnostic Test

To select the S-RAM diagnostic test, while viewing the Hardware Diagnostic Menu screen, press the “9” key.

The test initially displays the following warning: THIS TEST WILL CORRUPT DATA AND LOGS CURRENTLY IN BATTERY BACKED RAM ! ! !

To proceed with the test, press the “0” key and then the “ENTER” key. The test automatically tests all 512kb of S-RAM memory and, if no faults are found, Screen HD-9 (shown at the right) appears to indicate the controller has passed the test.

SCREEN HD-9

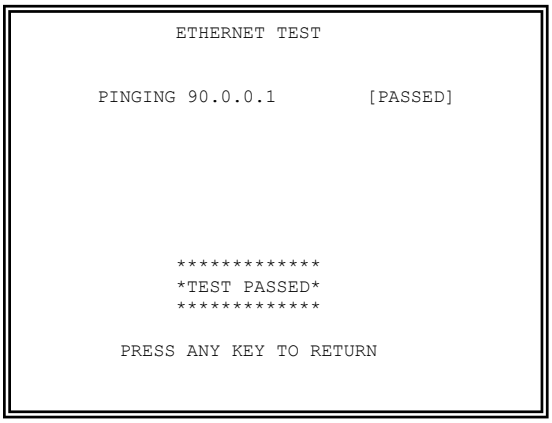


4.10.12. Ethernet Diagnostic Test

To successfully perform the Ethernet diagnostic test, the Ethernet connector (located at the upper left of the controller front panel and marked ETH) must be connected to a server. Of the two red LEDs located above the connector, the right LED should be steadily lighted and the left LED should blink three times as the test is performed.

To select the Ethernet diagnostic test, while viewing the Hardware Diagnostic Menu screen, press the “0” key. The test automatically “pings” the server three times and the server should respond. If successful, Screen HD-0 displays the “PASSED” result as shown at the right. If unsuccessful, the Screen HD-0 will display “FAILED.”

SCREEN HD-0



4.10.13. RTC/Other Diagnostic Test

To select the Real Time Clock RTC/Other diagnostic test, while viewing the Diagnostic Menu screen, press the SPEC FUNC key followed by the "1" key appropriate for the "A" character. When run, this test auto-performs a series of tests that check:

The controller's operating temp. (example: TEMP = 28.9).

The battery's output voltage (example: BATT = 3.0V).

The RTC firmware revision (example: FW rev = 10000).

Takes two readings of the RTC time to ensure the clock is running properly.

Tests the line frequency for accuracy.

Tests CVM/FM signals for proper function.

Screen HD-A (shown below) should appear to indicate the controller has passed the test or to indicate any failures.

SCREEN HD-A

```
RTC/OTHER TESTS

  GETTING TIME    [PASSED]
  GETTING TIME    [PASSED]
CLOCK IS RUNNING  [PASSED]
TESTING LINE FREQ. [PASSED]
TESTING CVM/FM SIGS. [PASSED]



*************
*TEST PASSED*
*************

PRESS ANY KEY TO RETURN
```

4.10.14. Data Module Diagnostic Test

To successfully perform the Data Module diagnostic test, a Datakey™ must be installed in the front panel Datakey™ receptacle.

To select the Datakey™ diagnostic test while viewing the Diagnostic Menu screen, press the SPEC FUNC key followed by the "2" key appropriate for the "B" character. When run, this test auto-performs a series of tests that check:

Formats the Datakey ™.

Performs an erasure check.

Writes a pattern to the flash block.

Performs a flash block read verification.

SCREEN HD-B

```
DATA MODULE TEST

FORMAT COMPLETE

CHECKING ERASURE  [PASSED]

READING FLASH BLOCK [PASSED]



*************
*TEST PASSED*
*************

PRESS ANY KEY TO RETURN
```

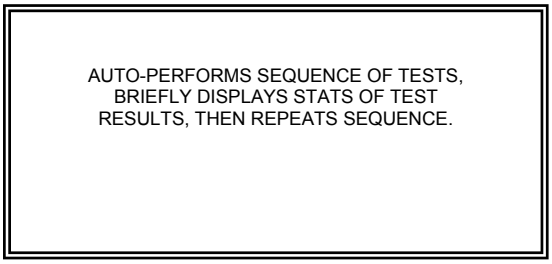
4.10.15. Auto-Loop Diagnostic Test

To successfully perform the Auto-Loop diagnostic test, all loopback cables

To select the Auto-Loop diagnostic test, while viewing the Diagnostic Menu screen, press the SPEC FUNC key followed by the “3” key appropriate for the “C” character.

When run, this test auto-performs the entire sequence of tests 1 through B, then briefly displays the statistics for the results before repeating the same sequence.

SCREEN HD-C



4.10.16. TS1 Suitcase Diagnostic Test

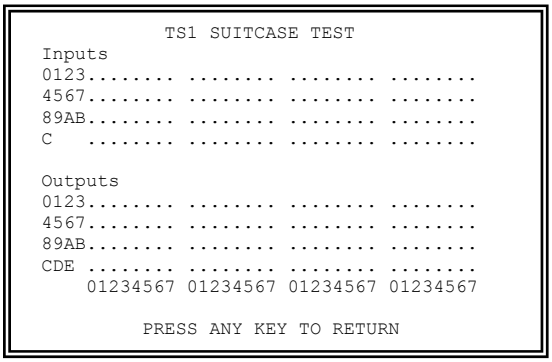
The TS1 Suitcase test allows the user to verify if controller inputs (as supplied by the suitcase tester) are operating correctly. Each input from the suitcase tester will display as an “X” if asserted, and displays a “.” (period) when not asserted.

The display position of the input under test is determined by the address of the input (see the table in Appendix H).

The display positions are organized in bytes, so the top line of display positions will display inputs 0x00 to 0x1F, the next line down will display inputs 0x20 to 0x3F, etc.

This test has no specific pass/fail criteria since it is intended for use as a troubleshooting tool only.

SCREEN HD-D



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5. TROUBLESHOOTING

5.1. Introduction

The fault isolation tables in this section list malfunctions and their possible causes. The list is by no means complete. However, careful study of the symptoms may provide a starting point for troubleshooting.

Because of the modular design of the ASC/3, repair at the cabinet level should be limited to removal and replacement of bad modules and fuses. Any in-depth fault isolation should be done in a shop with the proper test equipment. **Personnel and equipment should be properly grounded to prevent damage due to static electricity**. Exercise caution so that the programming integrity within the controller is maintained, as intended for the particular intersection, during removal and replacement of modules. Therefore, modules containing unique programming for a specific intersection (Processor module, overlap program board, Datakey$_{TM}$) must not be used operationally anywhere other than at that intersection.

If a problem is found on the Main CPU module or the I/O Connector Module, the customer has the option to either repair the equipment or return it to Econolite for service. The Ethernet Module, User Interface and Power Supply modules should always be returned to Econolite for service. In any case, all information relevant to the failure must be recorded. If a defective module or the complete controller is returned for service, please send as much information as possible about the failure. Note the nature of the malfunction and details about the conditions affecting the controller at the time of failure. Try to reproduce the failure in a lab to determine the pattern, if any. Use these guidelines when documenting a failure.

Record:

a) All controller settings. Print all data, if possible.
b) Mode of operation (coordination, preemption, time base).
c) All external conditions (temperature, humidity, lightning,.
d) Time of failure.
e) Interconnect type.

Record details of a failure condition:

a) Controller hangs-up.
b) Record: The interval, how often hang-up occurs (every cycle, during a certain function,...).
c) Controller skips intervals.
d) Record: The interval, under what conditions (every cycle, only when external command is applied,...).

Use descriptive statements:

a) Local not responding.
b) Incorrect data in a readback.
c) Incorrect output at a local.
d) Abnormal LCD indications.
e) Improper signal indications on the same phase (conflicting conditions).

The fault isolation tables are preceded by some precautions. It is imperative that these be read and understood before attempting to work on the ASC/3 controller.

5.2. Precautions

Before doing any troubleshooting please note that much of the ASC/3 operation is determined by the program contained in the configuration database.

1. Make sure that the program number on the label on top of the controller matches the Standard Software number specified on SCREEN MM-8-5 of the system software.
2. If necessary, use the Software Install procedure (Programming Manual, Appendix G) to check the database against the required intersection configuration.

Before working on any module, ALWAYS take the following precautionary steps:

1. Disconnect primary power from the controller before removing or installing modules.
2. Allow at least 15 seconds for the filter capacitors to discharge before working on any module in the controller.
3. Do not use low resistance VOM or continuity tester for continuity checks. These may damage CMOS circuits.
4. Remember to handle the Processor module with care to ensure that the on-card battery is not inadvertently shorted (such as by laying the module on a metal surface) or bent.
5. Be careful not to flex the any module circuitry excessively. When bench testing, the module should be supported by a fixture so that it lays flat and does not rest on the capacitor mounted on the rear of the module.

****WARNING****

Line voltages are present on the Processor-I/O and Power Supply modules. Extreme care should be taken when working in these areas.

5.3. Hardware Fault Isolation

		In ACTION column: (A) = Cabinet-level fault isolation. (B) = Bench-level fault isolation.
PROBLEM	**POSSIBLE CAUSE**	**ACTION**
Controller is inoperative. Processor Monitor and All LEDs are OFF.	1. 115 VAC fuse blown. 2. Controller not supplied with 115 VAC. 3. Loose power supply harnesses 4. Power supply module failure	1. (A) Check fuse F2 replace if necessary. 2. (A) Verify that power is applied. 3. (B) Check construction and seating of harnesses. 4. (B) Verify +24VDC output. Return supply to Econolite for repair.
Time is lost when power removed. Timing incorrect or inconsistent or controller hangs up.	1. Battery jumper JP2 not on 120 Hz reference circuit. 2. U10/U11 circuit.	1. (A) Remove/replace Main CPU module. (B) Check AC power monitor LINESYNC circuit interrupt operation (U11 pin 19) [7,4,C]. 2. (A) Remove/replace CPU Main module. (B) Check U1 programming (C) Check U10 OPTO circuit [7,3,A]. (CAUTION: LETHAL VOLTAGES PRESENT IN THIS CIRCUIT).
Voltage monitor/ Fault monitor output FALSE	1. Power supply out of tolerance, voltage or voltage monitor control circuit failed. 2. a) Preemptor phases programmed not IN USE when preemptor becomes active. b) Preemption active during power outage.	1. A) Remove/replace power supply. B) Check +24VDC and voltage monitor circuits (U11) [7,3,A]. 2. (A) Program preemption phases IN USE (Recall data page PREEMPTOR Submenu).
One phase has no outputs.	1. I/O section failure. Output circuitry for phase in I/O Interface section failed. 2. Phase omitted in configuration PROM programming.	1. (A) Remove/replace I/O Connector Module. (B) Check output circuit operation for the particular output. 2. (A) Install correct program application. (B) Reprogram Database in order to correct phase omitted.
Controller appears to be operating but all outputs are OFF.	1. 24 V EXT fuse (F1) is blown. 2. I/O Connector Module failure.	1. (A) Check fuse F1. 2. (A) Remove/replace I/O Connector Module. 3. (A) Check IO_OUT_EN output enable on J8 pin 8. 4. (A) Check SPI_MOSI on J8 pin
All outputs from one phase or one output does not turn ON.	1. I/O section failure. Output driver failed.	1. (A) Remove/replace Processor-I/O module. (B) Check output latch and output driver for that phase.

		In ACTION column: (A) = Cabinet-level fault isolation. (B) = Bench-level fault isolation.
PROBLEM	**POSSIBLE CAUSE**	**ACTION**
All inputs inoperative.	1. I/O Interface section failure. 2. Processor section failed.	1. (A) Remove/replace I/O Connector Module. (B) Check serial shift register chain U1 to U14 [12,6,D]. 2. (A) Remove/replace I/O Connector Module. (B) Check the SPI_MISO signal on J8 pin 4.
All inputs to one phase or one input inoperative.	1. I/O Interface section failure. Input multiplexer failed. 2. Phase not IN USE.	1. (A) Remove/replace I/O Connector Module. (B) Check shift register operation for that particular phase. 2. (A) Program phase IN USE on Recall data page Controller Submenu.
No inputs or outputs from a phase	1. Phase not IN USE.	1. (A) Check Recall data page Controller Submenu.
Controller beeps repetitively. Does not accept keyboard inputs.	1. A key is stuck ON or the keyboard control circuit failed.	1. (A) Check User Interface control circuits.
Controller hangs up and PROCESSOR MONITOR LED LED1 is ON.	1. Processor failed. 2. Power supply failed.	1. (A) Remove/replace Main CPU Module. (B) Check processor operation. 2. (A) Remove/replace power supply. (B)Check power supply for low voltage output.
Characters are lost while printing.	1. XON / XOFF handshake protocol not recognized.	1. (A) Program printer to recognize XON / XOFF protocol.

6. APPENDIX A: SCHEMATIC DRAWINGS

Appendix Contents

Processor Module (Drawing 100-1013-601, Sheets 1-10)

User Interface Module (Drawing, Sheets 1-4)

Ethernet Schematic (Drawing 100-1006-601, Sheets 1-3)

ASC/3 TS2 Type 2 Interface (Drawing 100-1008-601 Sheets 1 -7)

ASC/3 Telemetry Main PCB (Drawing 100-1032-601, Sheets 1-6)

ASC/3 Telemetry Daughter Board, 9-Pin (Drawing 100-1091-601, Sheet 1)

ASC/3 Telemetry Daughter Board, 25-Pin (Drawing 100-1092-601, Sheet 1)

ASC/3 Telemetry Main PCB (Drawing 100-1093-601, Sheets 1-6)

ASC/3 RM Field I/O Interface Board (Drawing 100-1119-601)

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MPC862 Port Usage	
SCC1–PORT1 SDLC	CLK2,3
SCC2–PORT4 EXPANSION [SP1]	BRG0
SCC3–PORT2 TERMINAL	BRG1
SCC4–PORT5 EXPANSION [SP2/SP5]	BRG2
SMC1–PORT3A	BRG3
SMC2–TELEMETRY PORT3B	CLK1

MPC862 Chip Select/Memory Usage		
FLASH BOOT MEMORY [16 bit]	$\overline{CS0}$	0xFF80 0000
SDRAM MEMORY [32 bit]	$\overline{CS1}$	0x0000 0000
SRAM MEMORY [8 bit]	$\overline{CS2}$	0x0200 0000
Not Used	$\overline{CS3}$	---------
LCD DEVICE I/O [8 bit]	$\overline{CS4}$	0x0300 0000
KEYBOARD I/O [8 bit]	$\overline{CS5}$	0x0301 0000
GPIO INPUTS [8 bit]	$\overline{CS6}$	0x0302 0000
UART [8 bit]	$\overline{CS7}$	0x0303 0000
INTERNAL SFRS	---	0xFF00 0000

REVISION RECORD

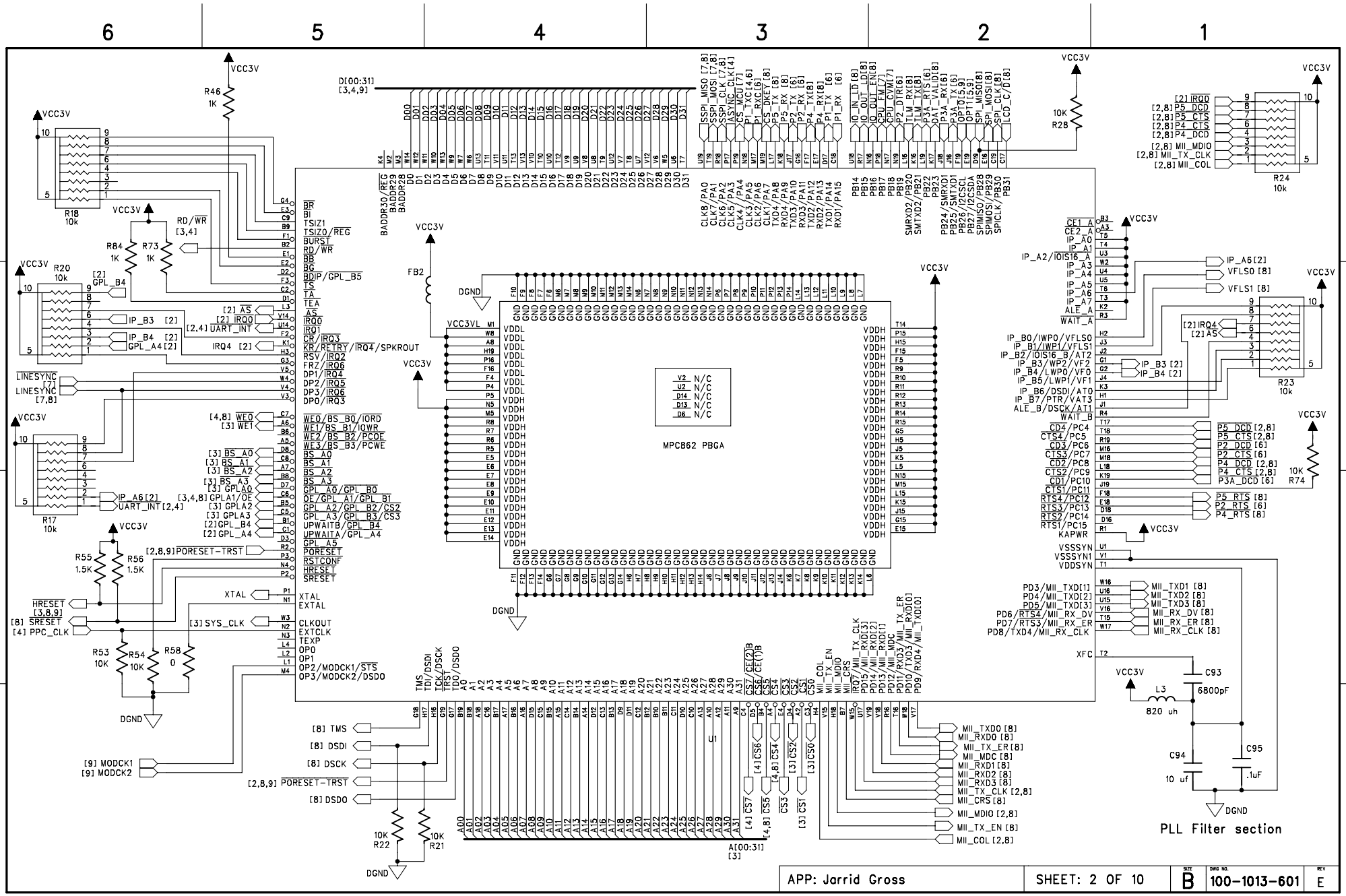
LTR	DESCRIPTION	APPROVED:	DATE:
NC	INITIAL RELEASE ECO # 21200	JARRID GROSS	7/27/04
A	SEE ECO # 21335	JARRID GROSS	10/26/04
B	SEE ECO # 21705		
C	SEE ECO # 21974	JIM ROSE	5/10/06
D	SEE ECO # 22135	JIM ROSE	9/8/06
E	SEE ECO # 22376	JIM ROSE	05/03/07

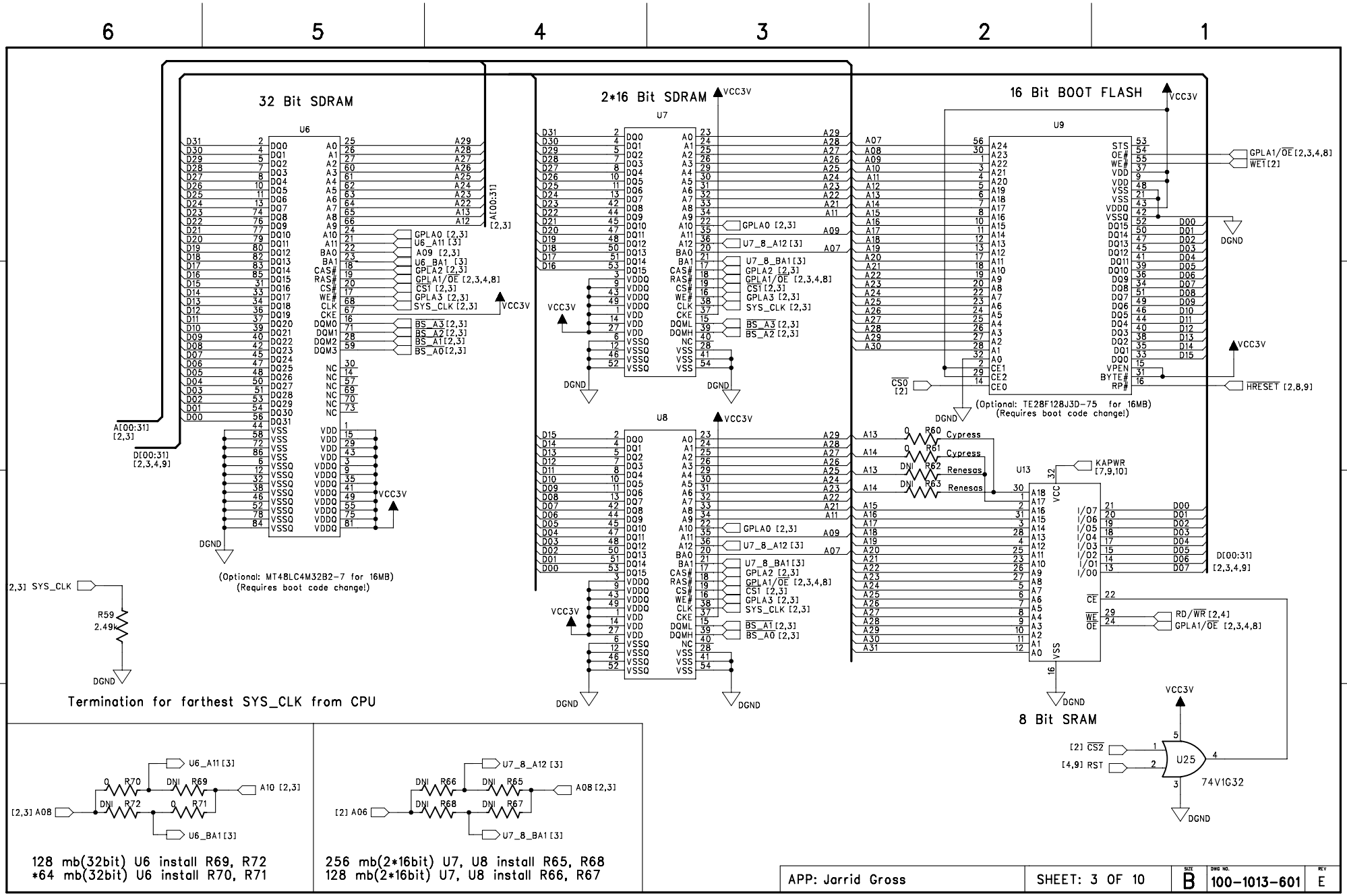
ECONOLITE CONTROL PRODUCTS INC
3360 E. LA PALMA AVE.
ANAHEIM, CALIFORNIA 92806

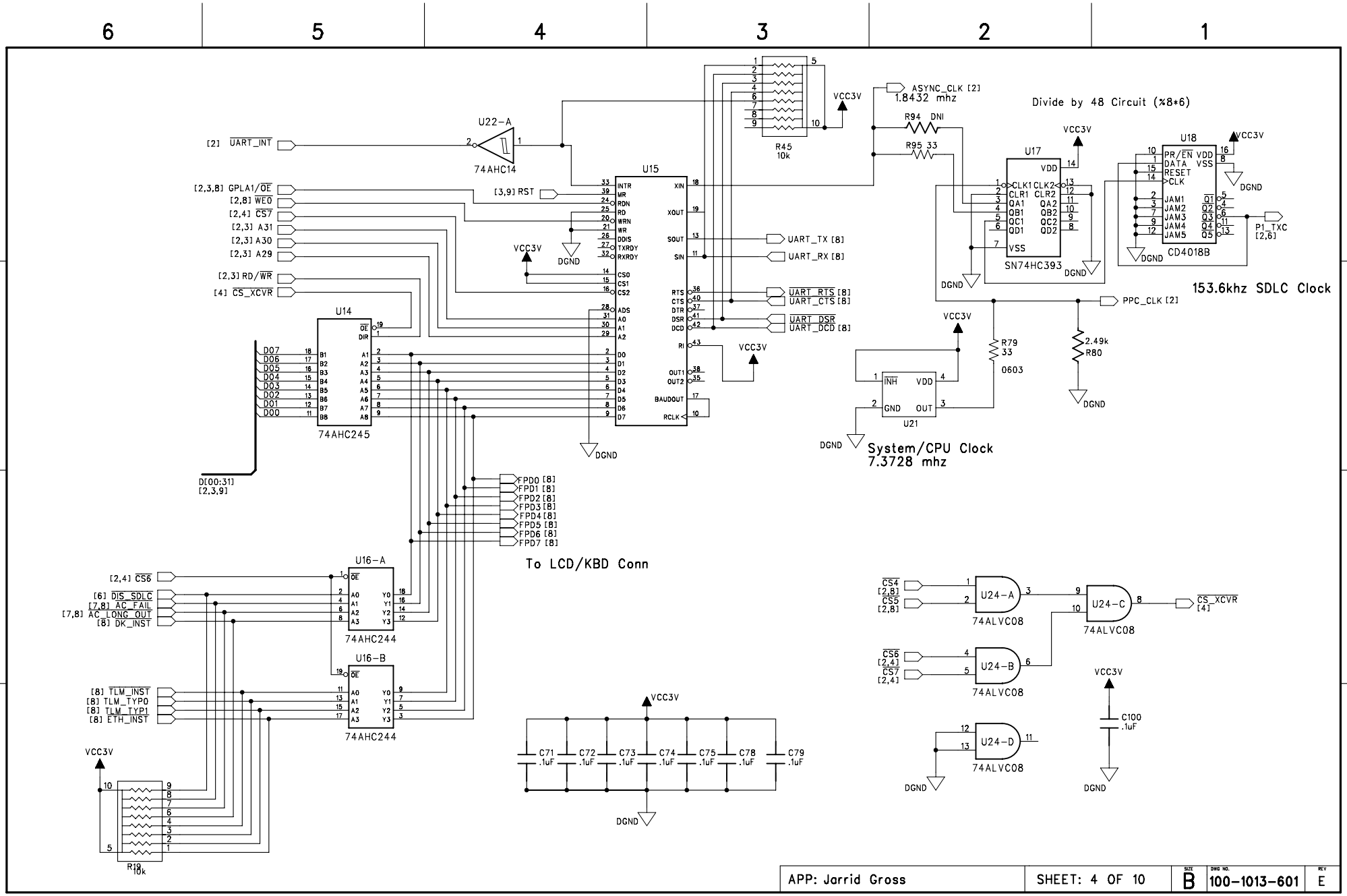
DR: Jarrid Gross	05-12-03
CHK: Jarrid Gross	07-16-04
ENG: Jarrid Gross	07-16-04
APP: Jarrid Gross	07-16-04

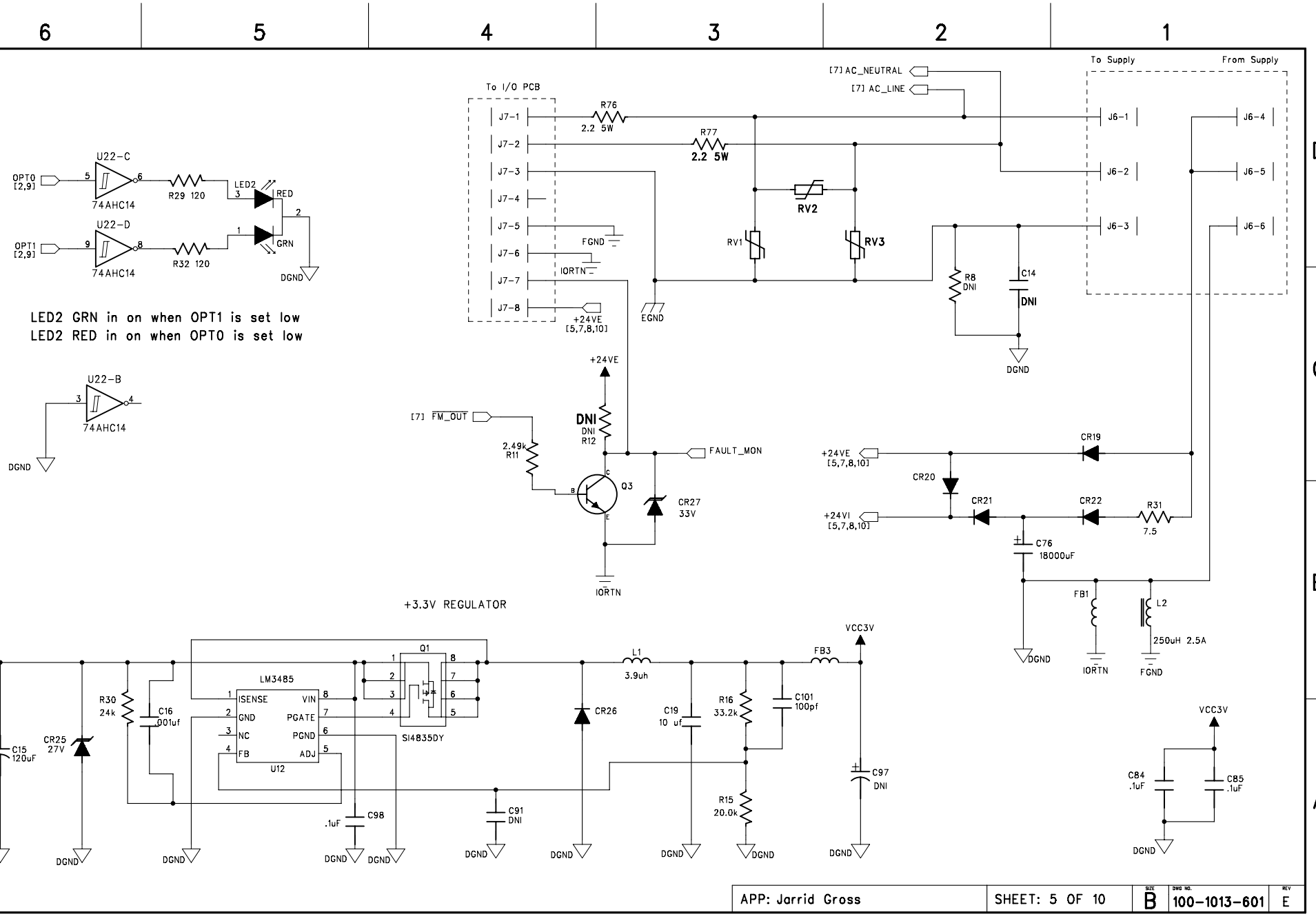
TITLE
SCHEMATIC
ASC III MAIN CONTROLLER

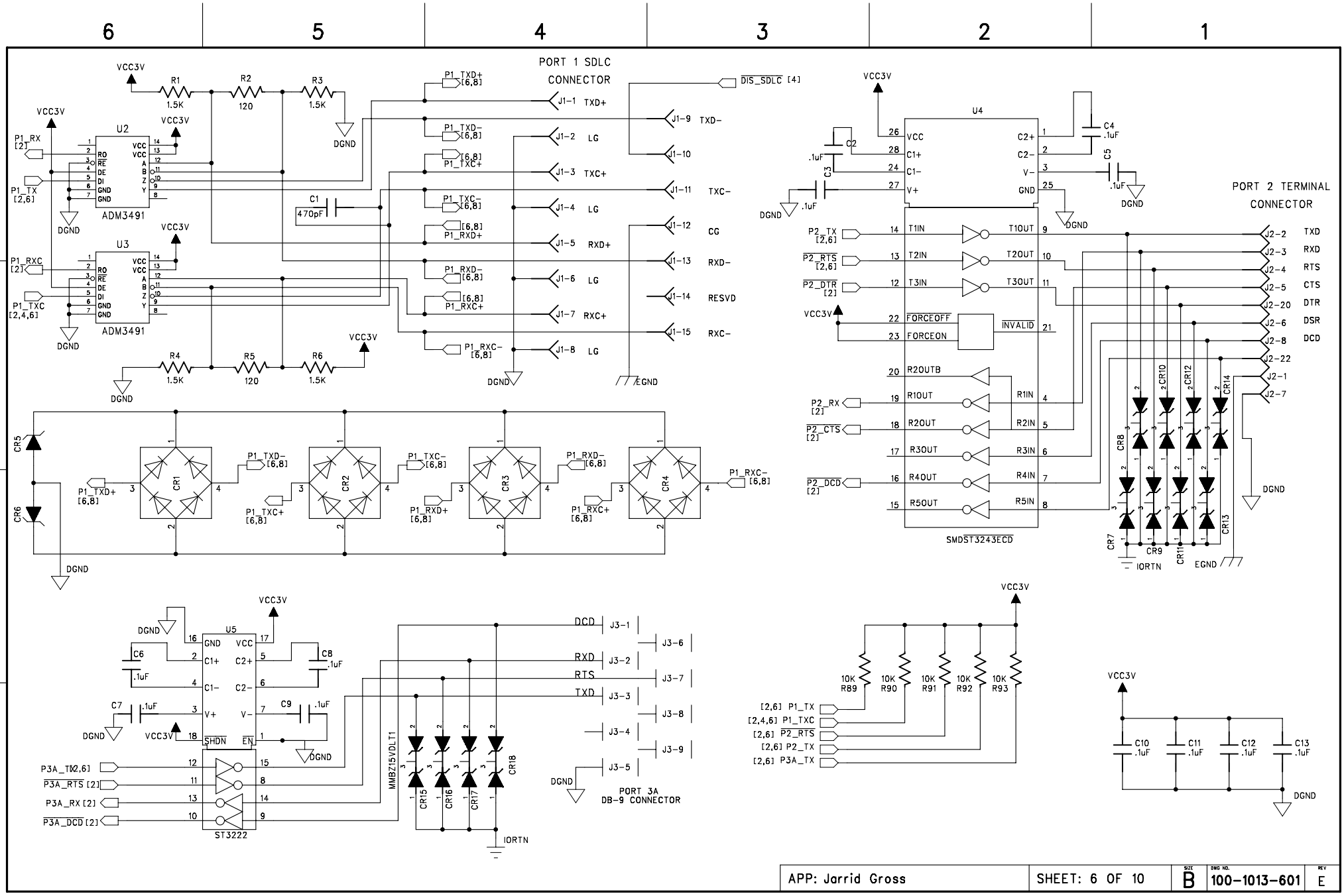
SHEET: 1 OF 10 | SIZE B | DWG NO. 100-1013-601 | REV E

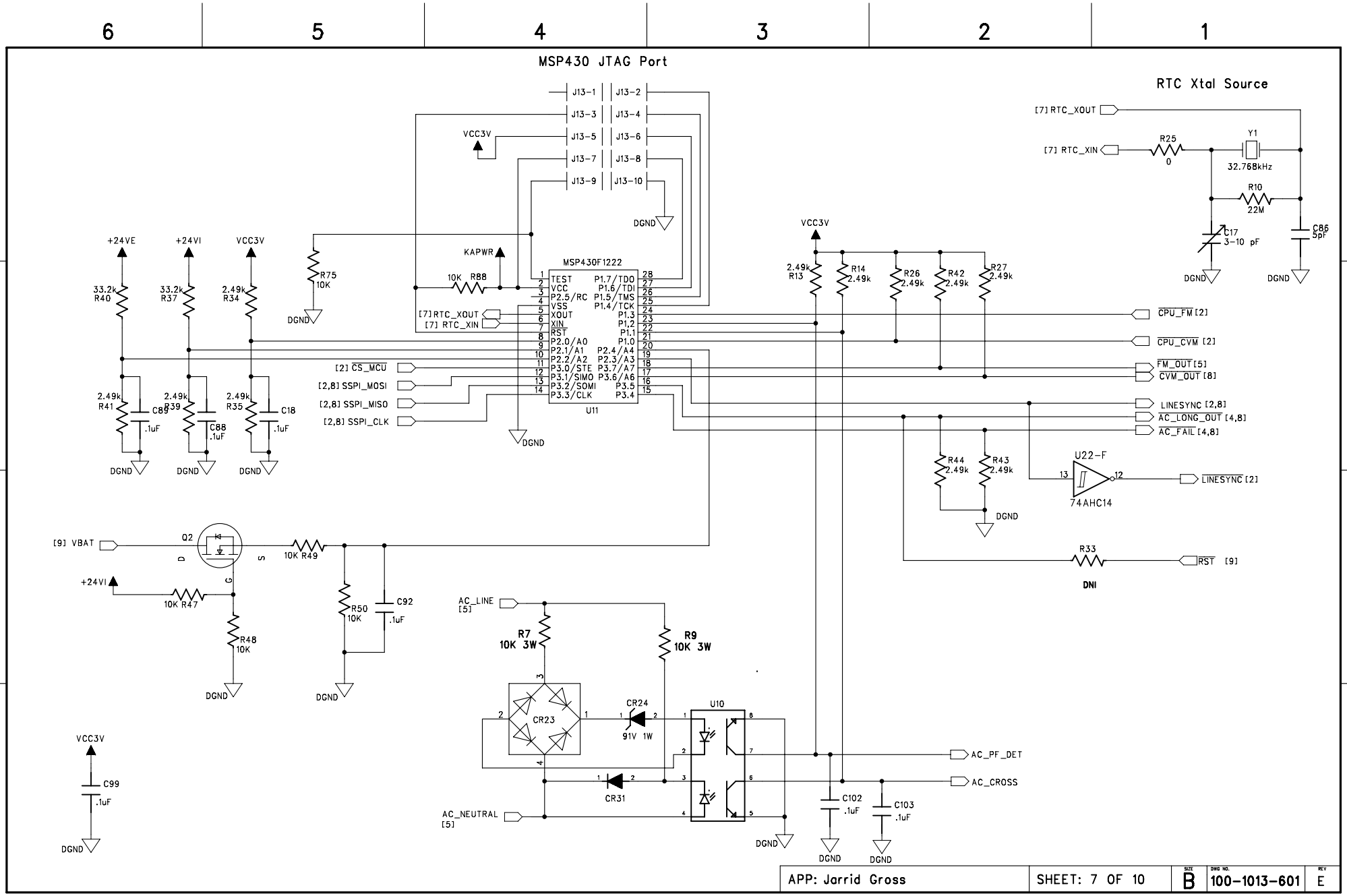

MPC862 PBGA
PLL Filter section
APP: Jarrid Gross
SHEET: 2 OF 10
B
100-1013-601
E

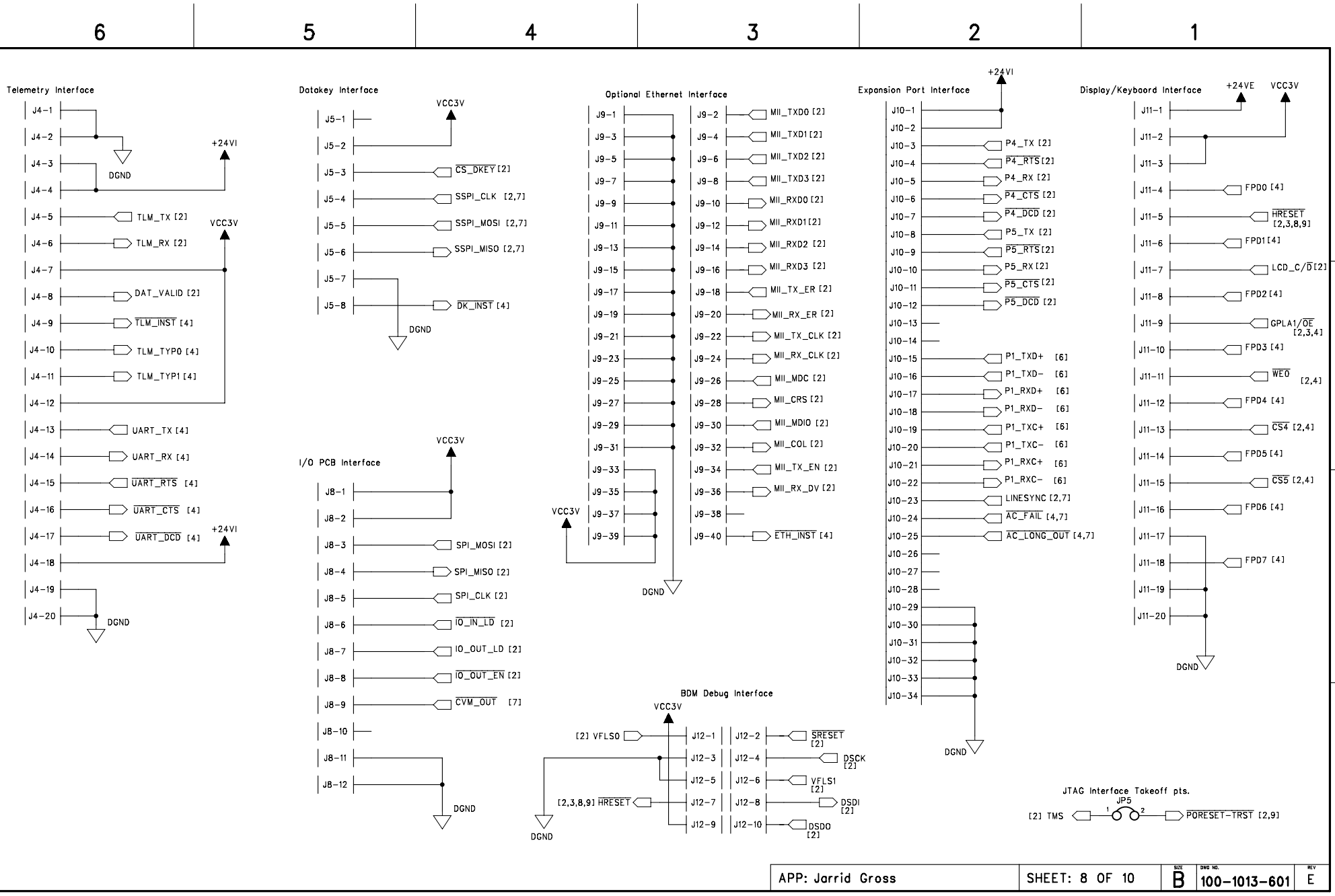

32 Bit SDRAM
2*16 Bit SDRAM
16 Bit BOOT FLASH
8 Bit SRAM
U6
U7
U8
U9
U13
U25
74V1G32
VCC3V
DGND
A[00:31] [2,3]
D[00:31] [2,3,4,9]
(Optional: MT48LC4M32B2-7 for 16MB)
(Requires boot code change!)
(Optional: TE28F128J3D-75 for 16MB)
(Requires boot code change!)
Termination for farthest SYS_CLK from CPU
2,3] SYS_CLK
R59
2.49K
128 mb(32bit) U6 install R69, R72
*64 mb(32bit) U6 install R70, R71
256 mb(2*16bit) U7, U8 install R65, R68
128 mb(2*16bit) U7, U8 install R66, R67
APP: Jarrid Gross
SHEET: 3 OF 10
SIZE B
DWG NO. 100-1013-601
REV E


6
5
4
3
2
1
D
C
B
A
U22-A
74AHC14
[2] UART_INT
U15
[3,9] RST
[2,3,8] GPLA1/OE
[2,8] WE0
[2,4] CS7
[2,3] A31
[2,3] A30
[2,3] A29
[2,3] RD/WR
[4] CS_XCVR
UART_TX [8]
UART_RX [8]
UART_RTS [8]
UART_CTS [8]
UART_DSR
UART_DCD [8]
R45
10k
VCC3V
DGND
U14
74AHC245
D[00:31]
[2,3,9]
FPD0 [8]
FPD1 [8]
FPD2 [8]
FPD3 [8]
FPD4 [8]
FPD5 [8]
FPD6 [8]
FPD7 [8]
To LCD/KBD Conn
U16-A
U16-B
74AHC244
[2,4] CS6
[6] DIS_SDLC
[7,8] AC_FAIL
[7,8] AC_LONG_OUT
[8] DK_INST
[8] TLM_INST
[8] TLM_TYP0
[8] TLM_TYP1
[8] ETH_INST
R19
10k
C71 .1uF
C72 .1uF
C73 .1uF
C74 .1uF
C75 .1uF
C78 .1uF
C79 .1uF
ASYNC_CLK [2]
1.8432 mhz
R94 DNI
R95 33
Divide by 48 Circuit (x8*6)
U17
SN74HC393
U18
CD4018B
153.6khz SDLC Clock
P1_TXC
[2,6]
PPC_CLK [2]
R79
33
0603
2.49k
R80
U21
System/CPU Clock
7.3728 mhz
U24-A
U24-B
U24-C
U24-D
74ALVC08
CS4
[2,8]
CS5
[2,8]
CS6
[2,4]
CS7
[2,4]
CS_XCVR
[4]
C100
.1uF
APP: Jarrid Gross
SHEET: 4 OF 10
B
100-1013-601
E

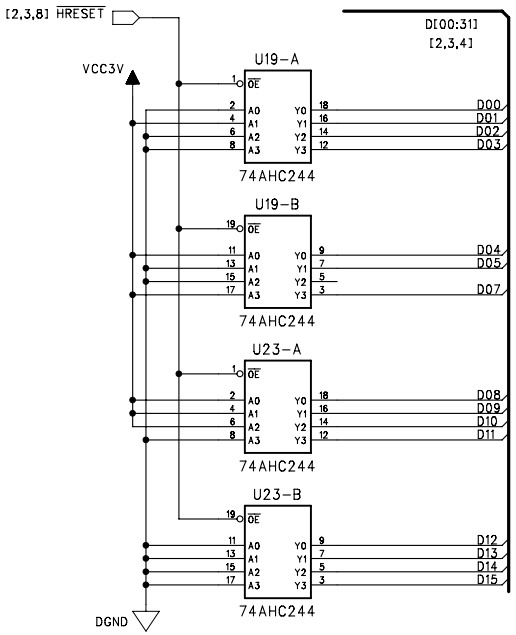

6
5
4
3
2
1
D
C
B
A
U22-C
OPT0 [2,9]
74AHC14
R29 120
LED2
RED
GRN
U22-D
OPT1 [2,9]
74AHC14
R32 120
DGND
LED2 GRN in on when OPT1 is set low
LED2 RED in on when OPT0 is set low
U22-B
74AHC14
DGND
To I/O PCB
J7-1
J7-2
J7-3
J7-4
J7-5
J7-6
J7-7
J7-8
R76
2.2 5W
R77
2.2 5W
RV2
RV1
RV3
FGND
IORTN
+24VE [5,7,8,10]
EGND
[7] AC_NEUTRAL
[7] AC_LINE
To Supply
From Supply
J6-1
J6-2
J6-3
J6-4
J6-5
J6-6
R8
DNI
C14
DNI
DGND
+24VE
[7] FM_OUT
DNI
DNI
R12
2.49k
R11
Q3
FAULT_MON
CR27
33V
IORTN
+24VE [5,7,8,10]
CR19
CR20
CR21
CR22
R31
7.5
+24VI [5,7,8,10]
C76
18000uF
FB1
L2
250uH 2.5A
DGND
IORTN
FGND
+3.3V REGULATOR
[5,7,8,10]
+24VI
C15
120uF
CR25
27V
R30
24k
C16
.001uf
LM3485
ISENSE
GND
NC
FB
VIN
PGATE
PGND
ADJ
U12
Q1
SI4835DY
C98
.1uF
C91
DNI
CR26
L1
3.9uh
C19
10 uf
R16
33.2k
C101
100pf
R15
20.0k
FB3
VCC3V
C97
DNI
C84
.1uF
C85
.1uF
DGND
APP: Jarrid Gross
SHEET: 5 OF 10
SIZE
B
DWG NO.
100-1013-601
REV
E


PORT 1 SDLC CONNECTOR
PORT 2 TERMINAL CONNECTOR
PORT 3A DB-9 CONNECTOR
ADM3491
SMDST3243ECD
ST3222
MMBZ15VDLT1
APP: Jarrid Gross
SHEET: 6 OF 10
SIZE B
DWG NO. 100-1013-601
REV E

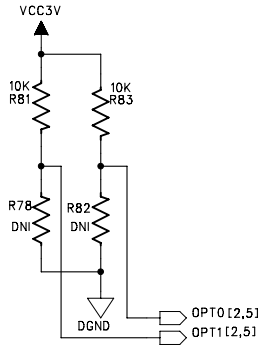

MSP430 JTAG Port
RTC Xtal Source
J13-1
J13-2
J13-3
J13-4
J13-5
J13-6
J13-7
J13-8
J13-9
J13-10
VCC3V
DGND
KAPWR
MSP430F1222
TEST
VCC
P2.5/RC
VSS
XOUT
XIN
RST
P2.0/A0
P2.1/A1
P2.2/A2
P3.0/STE
P3.1/SIMO
P3.2/SOMI
P3.3/CLK
P1.7/TDO
P1.6/TDI
P1.5/TMS
P1.4/TCK
P1.3
P1.2
P1.1
P1.0
P2.4/A4
P2.3/A3
P3.7/A7
P3.6/A6
P3.5
P3.4
U11
[7] RTC_XOUT
[7] RTC_XIN
[2] CS_MCU
[2,8] SSPI_MOSI
[2,8] SSPI_MISO
[2,8] SSPI_CLK
+24VE
+24VI
33.2k R40
33.2k R37
2.49k R34
2.49k R41
2.49k R39
2.49k R35
C89 .1uF
C88 .1uF
C18 .1uF
R75 10K
10K R88
2.49k R13
R14 2.49k
R26 2.49k
R42 2.49k
R27 2.49k
CPU_FM [2]
CPU_CVM [2]
FM_OUT [5]
CVM_OUT [8]
LINESYNC [2,8]
AC_LONG_OUT [4,8]
AC_FAIL [4,8]
R44 2.49k
R43 2.49k
U22-F
74AHC14
LINESYNC [2]
R33
DNI
RST [9]
[7] RTC_XOUT
[7] RTC_XIN
R25 0
Y1 32.768kHz
R10 22M
C17 3-10 pF
C86 5pF
[9] VBAT
Q2
10K R49
10K R47
R48 10K
R50 10K
C92 .1uF
AC_LINE [5]
R7 10K 3W
R9 10K 3W
CR23
CR24
91V 1W
CR31
U10
AC_PF_DET
AC_CROSS
AC_NEUTRAL [5]
C102 .1uF
C103 .1uF
C99 .1uF
APP: Jarrid Gross
SHEET: 7 OF 10
SIZE B
DWG NO. 100-1013-601
REV E


6
5
4
3
2
1
D
C
B
A
Telemetry Interface
J4-1
J4-2
J4-3
J4-4
J4-5
J4-6
J4-7
J4-8
J4-9
J4-10
J4-11
J4-12
J4-13
J4-14
J4-15
J4-16
J4-17
J4-18
J4-19
J4-20
DGND
+24VI
VCC3V
TLM_TX [2]
TLM_RX [2]
DAT_VALID [2]
TLM_INST [4]
TLM_TYP0 [4]
TLM_TYP1 [4]
UART_TX [4]
UART_RX [4]
UART_RTS [4]
UART_CTS [4]
UART_DCD [4]
+24VI
DGND
Datakey Interface
J5-1
J5-2
J5-3
J5-4
J5-5
J5-6
J5-7
J5-8
VCC3V
CS_DKEY [2]
SSPI_CLK [2,7]
SSPI_MOSI [2,7]
SSPI_MISO [2,7]
DK_INST [4]
DGND
I/O PCB Interface
J8-1
J8-2
J8-3
J8-4
J8-5
J8-6
J8-7
J8-8
J8-9
J8-10
J8-11
J8-12
VCC3V
SPI_MOSI [2]
SPI_MISO [2]
SPI_CLK [2]
IO_IN_LD [2]
IO_OUT_LD [2]
IO_OUT_EN [2]
CVM_OUT [7]
DGND
Optional Ethernet Interface
J9-1
J9-2
J9-3
J9-4
J9-5
J9-6
J9-7
J9-8
J9-9
J9-10
J9-11
J9-12
J9-13
J9-14
J9-15
J9-16
J9-17
J9-18
J9-19
J9-20
J9-21
J9-22
J9-23
J9-24
J9-25
J9-26
J9-27
J9-28
J9-29
J9-30
J9-31
J9-32
J9-33
J9-34
J9-35
J9-36
J9-37
J9-38
J9-39
J9-40
VCC3V
DGND
MII_TXD0 [2]
MII_TXD1 [2]
MII_TXD2 [2]
MII_TXD3 [2]
MII_RXD0 [2]
MII_RXD1 [2]
MII_RXD2 [2]
MII_RXD3 [2]
MII_TX_ER [2]
MII_RX_ER [2]
MII_TX_CLK [2]
MII_RX_CLK [2]
MII_MDC [2]
MII_CRS [2]
MII_MDIO [2]
MII_COL [2]
MII_TX_EN [2]
MII_RX_DV [2]
ETH_INST [4]
BDM Debug Interface
VCC3V
[2] VFLS0
[2,3,8,9] HRESET
J12-1
J12-2
J12-3
J12-4
J12-5
J12-6
J12-7
J12-8
J12-9
J12-10
SRESET [2]
DSCK [2]
VFLS1 [2]
DSDI [2]
DSDO [2]
DGND
Expansion Port Interface
+24VI
J10-1
J10-2
J10-3
J10-4
J10-5
J10-6
J10-7
J10-8
J10-9
J10-10
J10-11
J10-12
J10-13
J10-14
J10-15
J10-16
J10-17
J10-18
J10-19
J10-20
J10-21
J10-22
J10-23
J10-24
J10-25
J10-26
J10-27
J10-28
J10-29
J10-30
J10-31
J10-32
J10-33
J10-34
DGND
P4_TX [2]
P4_RTS [2]
P4_RX [2]
P4_CTS [2]
P4_DCD [2]
P5_TX [2]
P5_RTS [2]
P5_RX [2]
P5_CTS [2]
P5_DCD [2]
P1_TXD+ [6]
P1_TXD- [6]
P1_RXD+ [6]
P1_RXD- [6]
P1_TXC+ [6]
P1_TXC- [6]
P1_RXC+ [6]
P1_RXC- [6]
LINESYNC [2,7]
AC_FAIL [4,7]
AC_LONG_OUT [4,7]
Display/Keyboard Interface
+24VE
VCC3V
J11-1
J11-2
J11-3
J11-4
J11-5
J11-6
J11-7
J11-8
J11-9
J11-10
J11-11
J11-12
J11-13
J11-14
J11-15
J11-16
J11-17
J11-18
J11-19
J11-20
DGND
FPD0 [4]
HRESET [2,3,8,9]
FPD1 [4]
LCD_C/D [2]
FPD2 [4]
GPLA1/OE [2,3,4]
FPD3 [4]
WE0 [2,4]
FPD4 [4]
CS4 [2,4]
FPD5 [4]
CS5 [2,4]
FPD6 [4]
FPD7 [4]
JTAG Interface Takeoff pts.
JP5
[2] TMS
PORESET-TRST [2,9]
APP: Jarrid Gross
SHEET: 8 OF 10
SIZE
B
DWG NO.
100-1013-601
REV
E

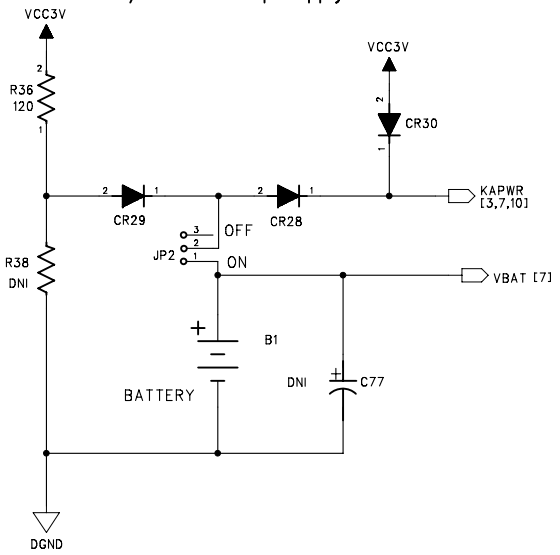
Config Word = 0b0000 0111 1001 0010
D06 intensionally left from data bus(rsvd)

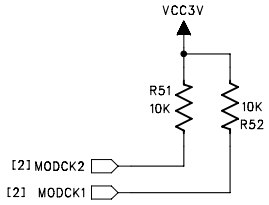


Assembly Options Selection	
Assembly Option	OPT-2,1,0
64mb 32bit SDRAM	X11
128 mb 32bit SDRAM	X01
128 mb 2X16bit SDRAM	X10
256 mb 2X16bit SDRAM	X00

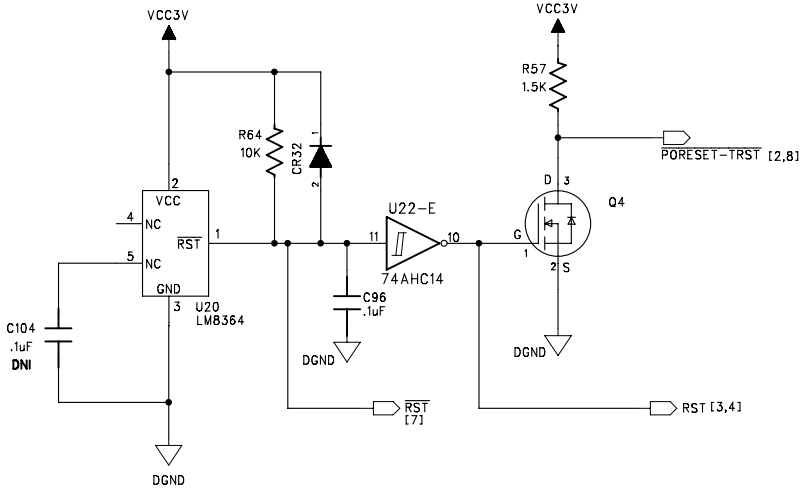


RTC/SRAM Backup supply





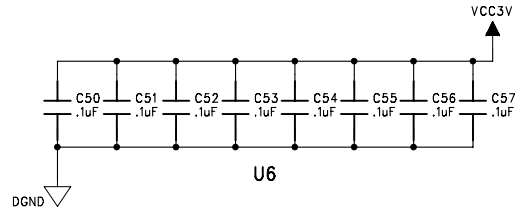
Power On Reset



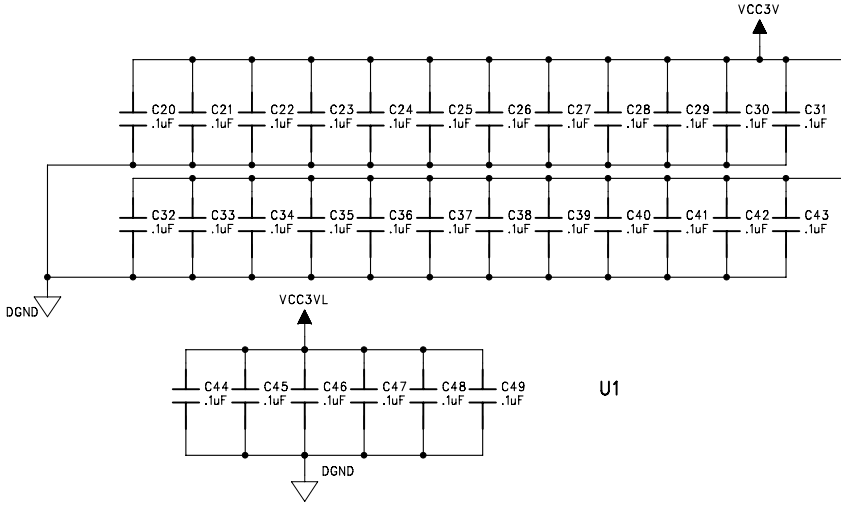
D0 = 0, Internal Arbitration
D1 = IIP, 1
D2 = 0, Boot Burst Disabled
D3 = 0, Boot Memory Match All
D[4,5] = 10, 16 bit port size
D6 = Reserved N/C
D[7,8] = 11, Internal Stack Base = 0xFFF00000
D[9,10] = 11, Debug pins as Debug
D[11,12] = 00, BDM Debug Mode
D[13,14] = 00, CLKOUT = full speed
D15 = 0, Core is Big Endian

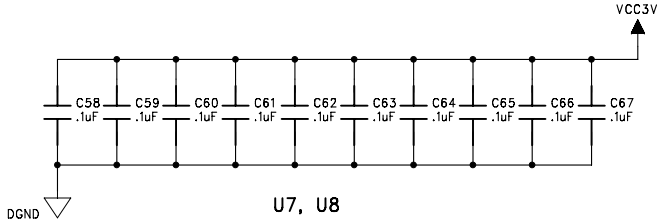
Boot Clock Config = 0b11 "MF=5, extclk"

APP: Jarrid Gross	SHEET: 9 OF 10	SIZE B	DWG NO. 100-1013-601	REV E

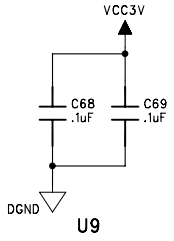


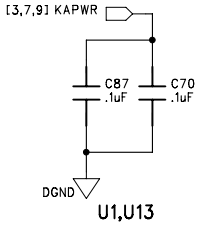
When U7, U8 are used, C50 to C57 are omitted

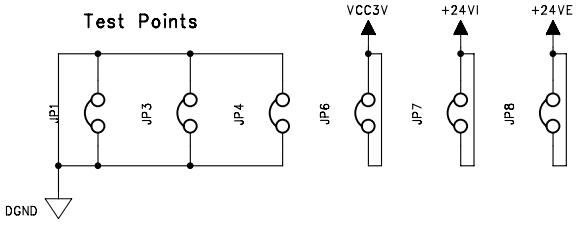


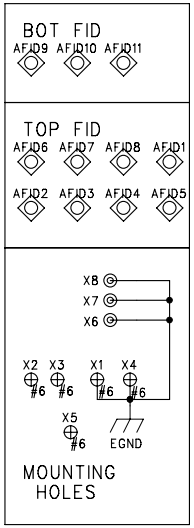


When U6 is used, C58 to C67 are omitted









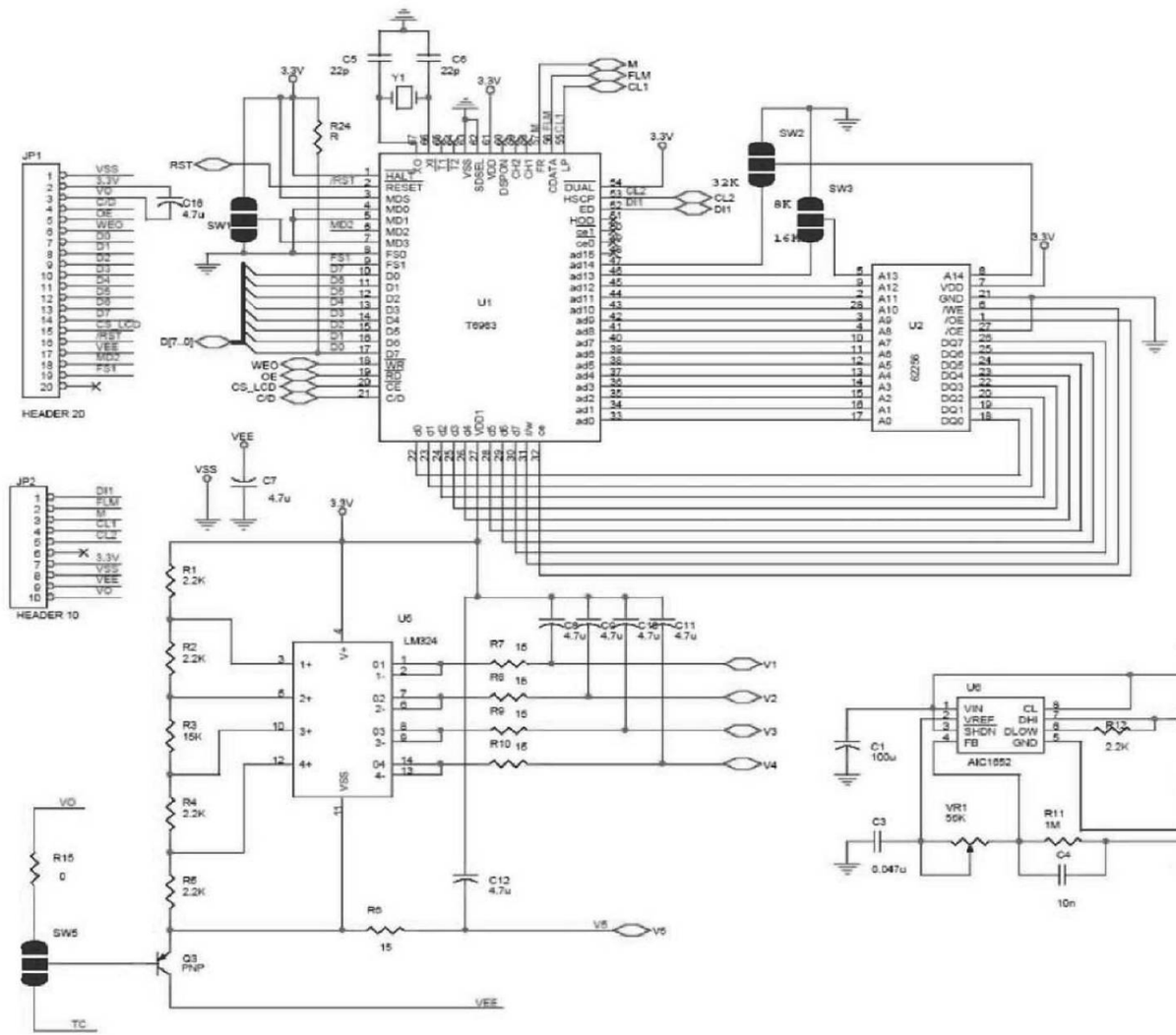
APP: Jarrid Gross	SHEET: 10 OF 10	SIZE B	DWG NO. 100-1013-601	REV E

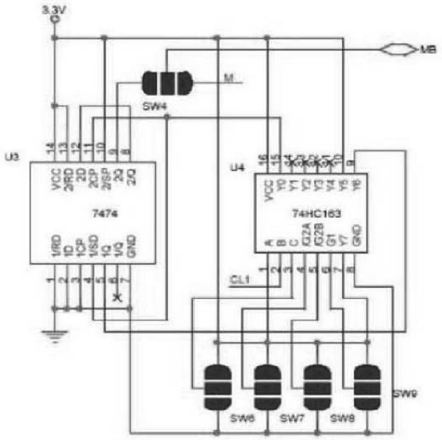
User Interface Module (Drawing- Sheets 1-4)

2 1

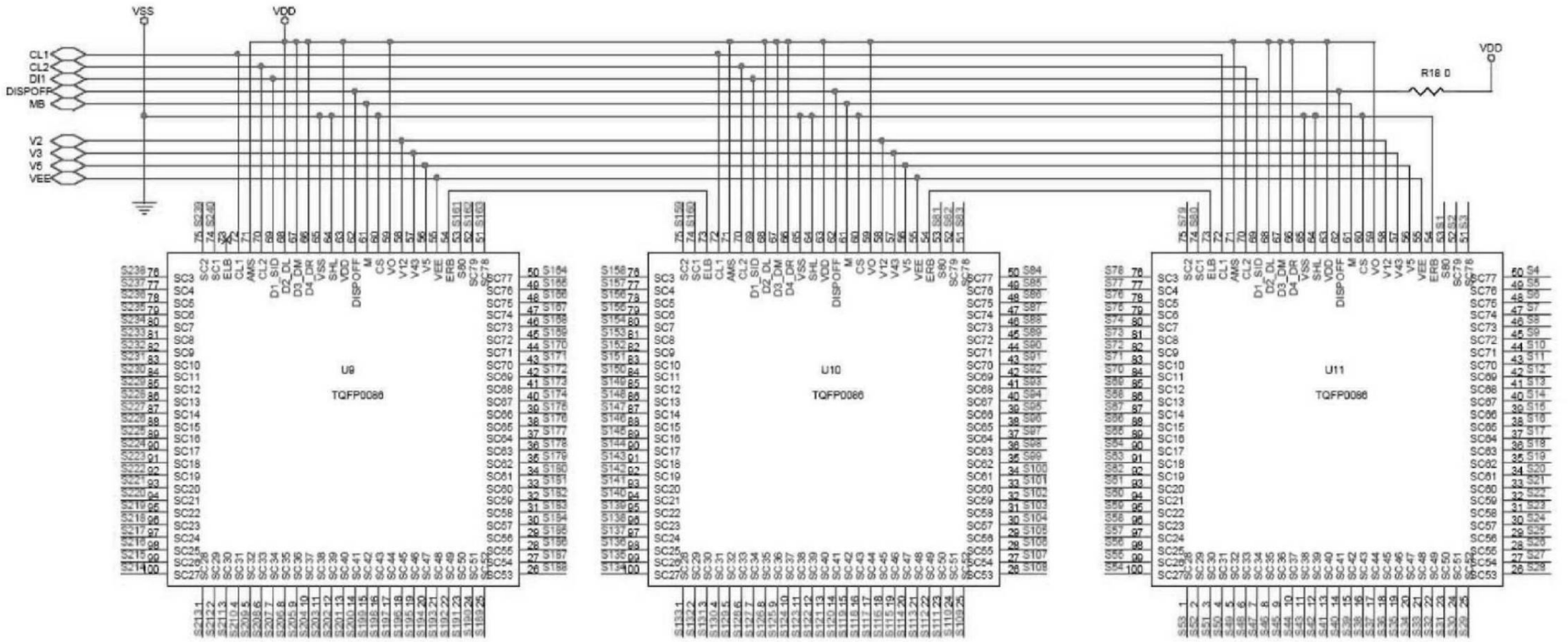
NOTES: (UNLESS OTHERWISE SPECIFIED)

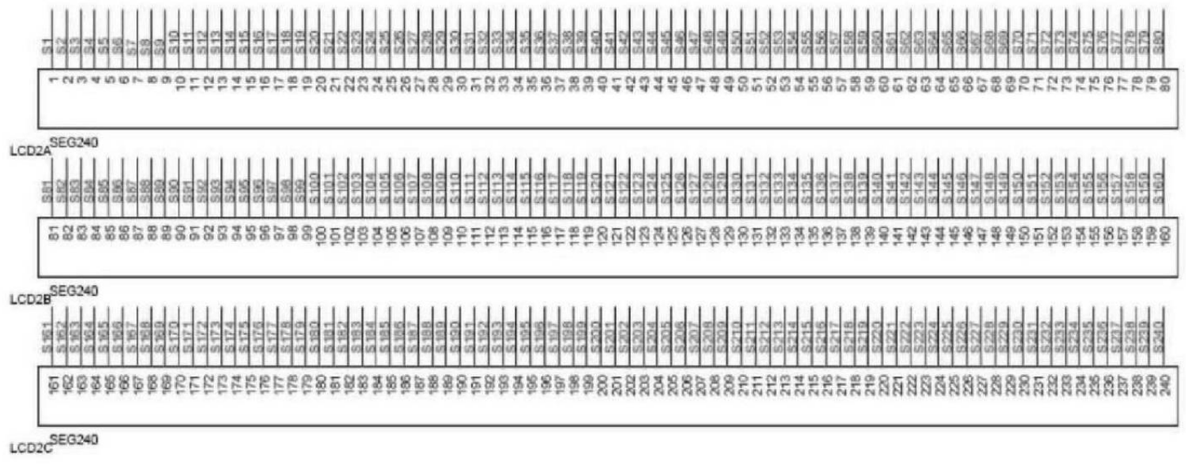
REVISIONS				
REV.	BY	E.C.O. NUMBER	DATE	APPRD





UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DEBURR AND BREAK ALL SHARP EDGES PART MUST BE FREE OF ANY FOREIGN CONTAMINANTS TOLERANCE DECIMAL: XX ± .03 XXX ± .015 ANGULAR: ± 0°30' This drawing is the property of ECONOLITE CONTROL PRODUCTS who claims proprietary rights in the material disclosed. It is issued in confidence for engineering information only and may not be copied or used for manufacture on anything shown without specific written permission from ECONOLITE CONTROL PRODUCTS.	DRAWN XXX	XXX	ECONOLITE CONTROL PRODUCTS, INC. 3360 E. La PALMA, ANAHEIM, CA. 92806
	DESIGN XXX	XXX	TITLE XXX XXX
	CHECK XXX	XXX	
	ENGINEER XXX	XXX	
	APPRD XXX	XXX	
	MATERIAL XXX XXX		SIZE B · CAGE CODE 0FEW7 · DRAWING NO. Draw1 · REV. 1
MODEL FILE: .SLDPRT	FINISH XXX XXX	DO NOT SCALE DRAWING	SCALE: 1:1 · CAD FILE: Draw1.SLDDRW · Sheet 1 OF 4





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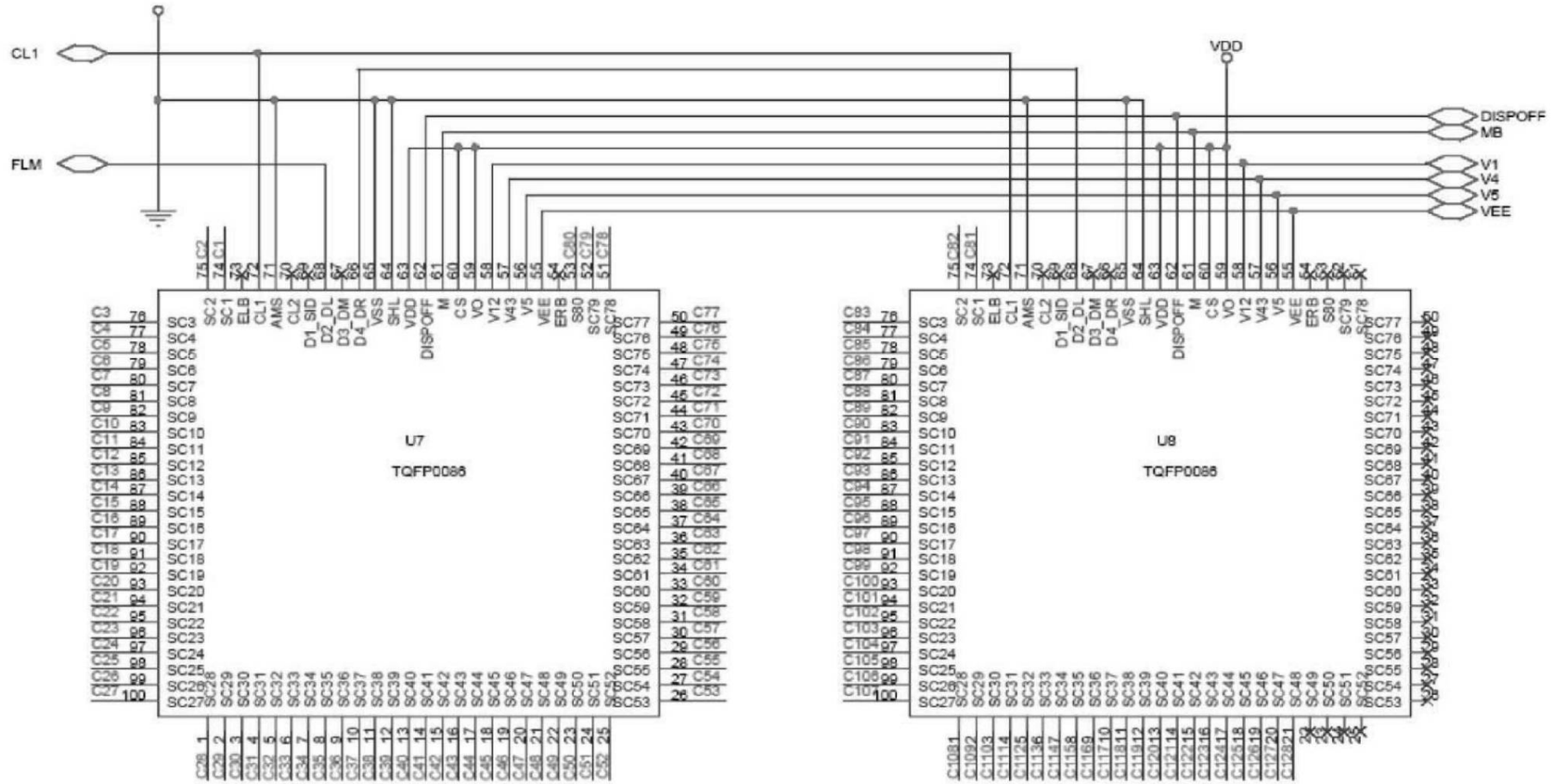
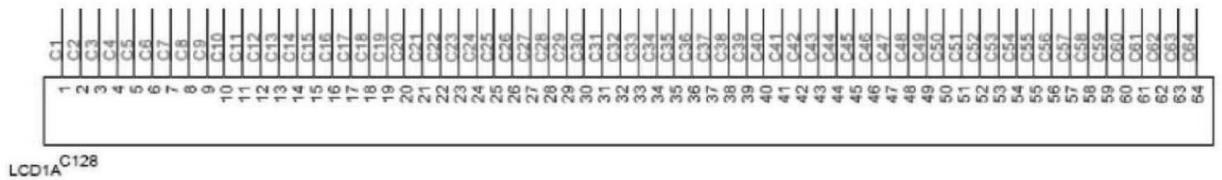
XXX
XXX

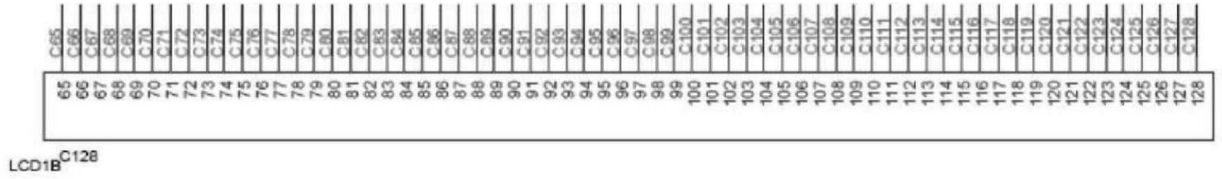
DO NOT SCALE DRAWING

SIZE	CAGE CODE	DRAWING NO.	REV.
B	OFEW7	Draw1	1

SCALE: 1:1	CAD FILE: Draw1.SLDDRW	SHEET 2 OF 4





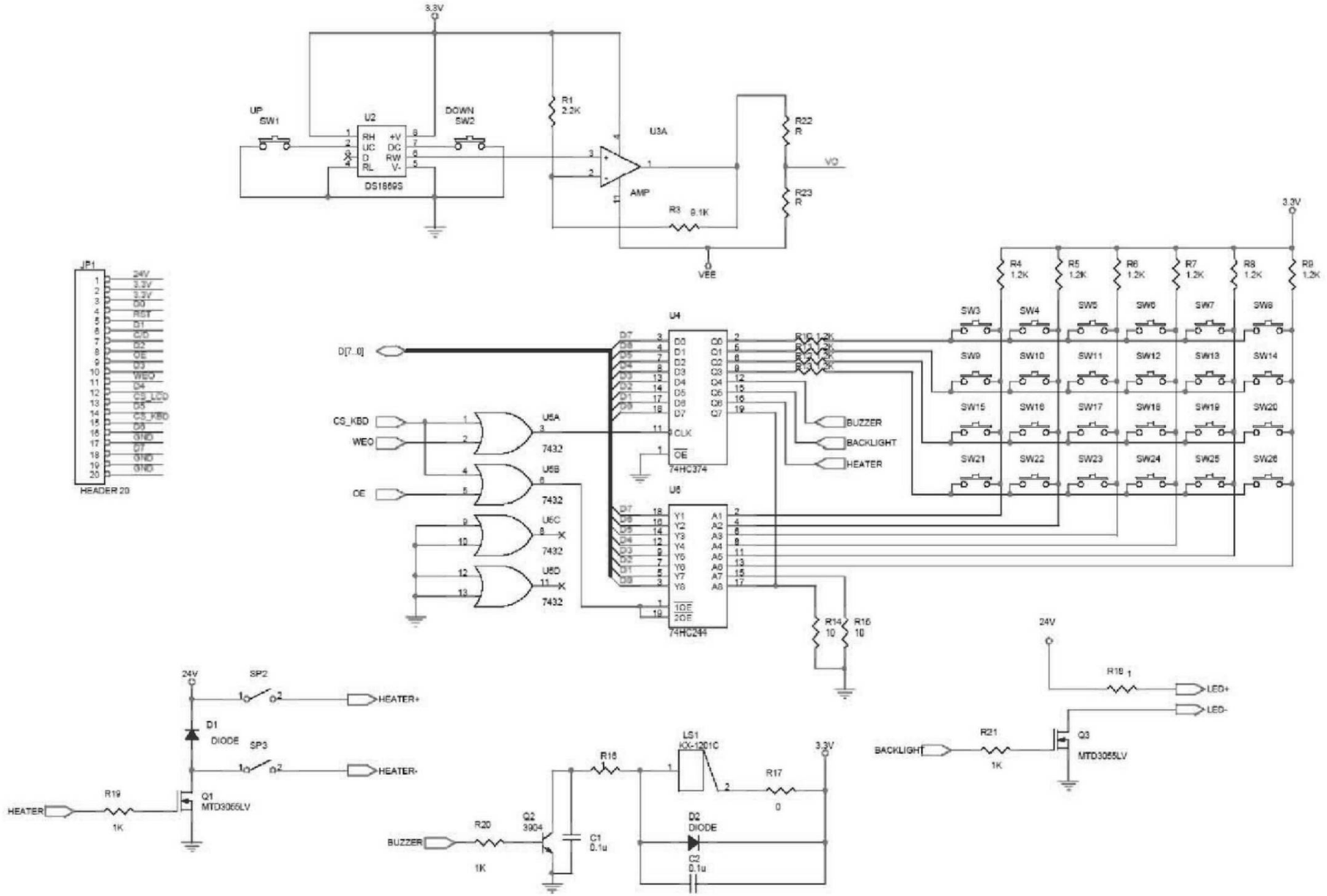


ECONOLITE
CONTROL PRODUCTS, INC.
3360 E. La PALMA ANAHEIM, CA 92806

XXX
XXX

DO NOT SCALE DRAWING

SIZE	CAGE CODE	DRAWING NO.	REV.
B	0FEW7	Draw1	1
SCALE: 1:1	CAD FILE: Draw1.SLDDRW	SHEET 3 OF 4	



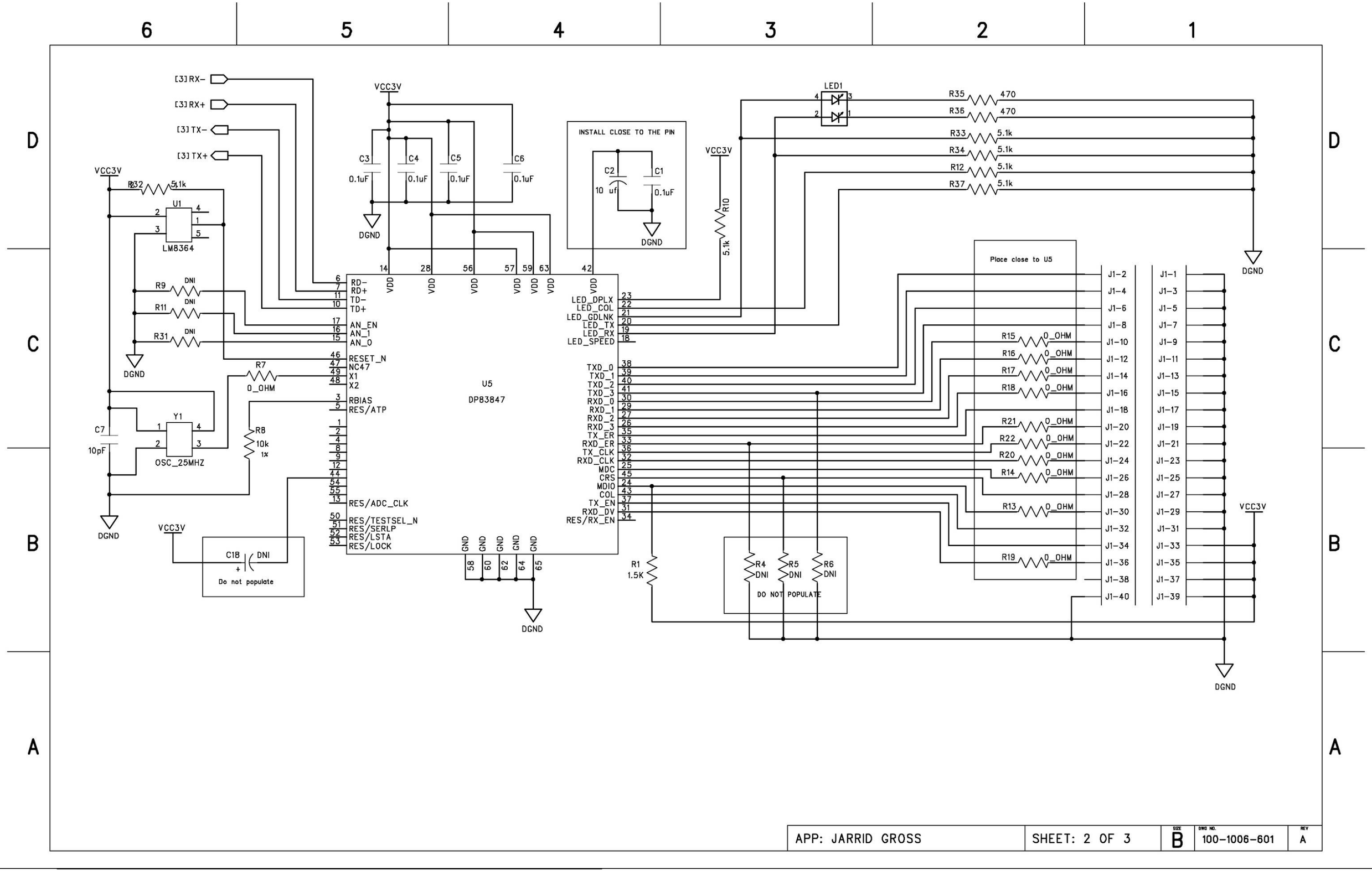
ECONOLITE CONTROL PRODUCTS, INC.	
3360 E. La PALMA ANAHEIM, CA 92806	
XXX XXX	
DO NOT SCALE DRAWING	
SIZE: B	CAGE CODE: 0FEW7
DRAWING NO.: Draw1	REV.: 1
SCALE: 1:1	CAD FILE: Draw1.SLDDRW
SHEET 4 OF 4	

100-1006-601a.sch-1 - Tue Feb 01 13:17:39 2005

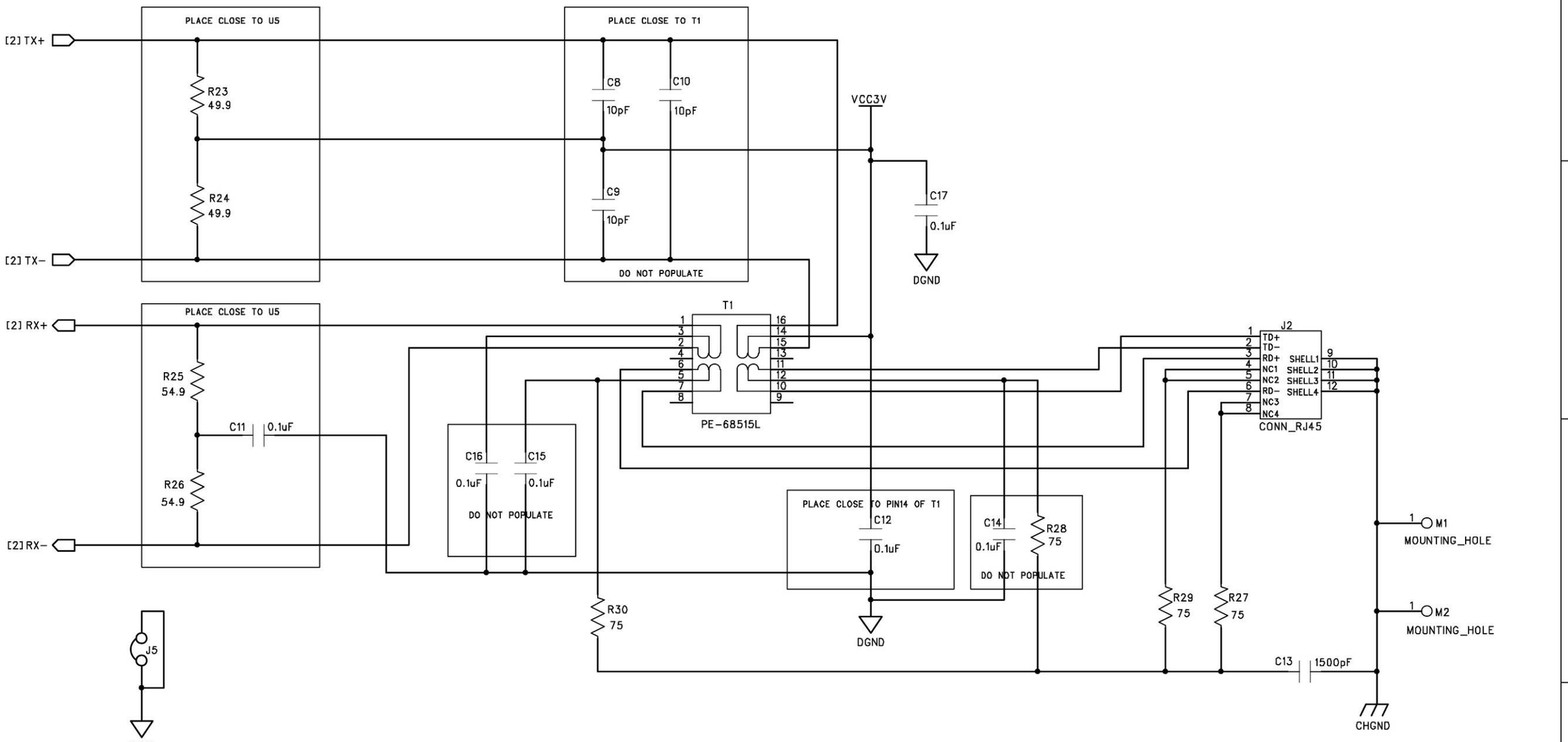
REVISION RECORD			
LTR	DESCRIPTION	APPROVED:	DATE:
NC	INITIAL RELEASE ECO# 21200	JARRID GROSS	7/27/04
A	SEE ECO#21427	JARRID GROSS	1/25/05

ECONOLITE CONTROL PRODUCTS INC
3360 E. LA PALMA AVE.
ANAHEIM, CALIFORNIA 92806

DR: WON LEE	10-8-02	TITLE: SCHEMATIC ETHERNET MODULE ASCIII			
CHK: JARRID GROSS	7-16-04				
ENG: JARRID GROSS	7-16-04				
APP: JARRID GROSS	7-16-04	SHEET: 1 OF 3	SIZE: B	DWG NO.: 100-1006-601	REV: A



APP: JARRID GROSS	SHEET: 2 OF 3	SIZE B	DWG NO. 100-1006-601	REV A



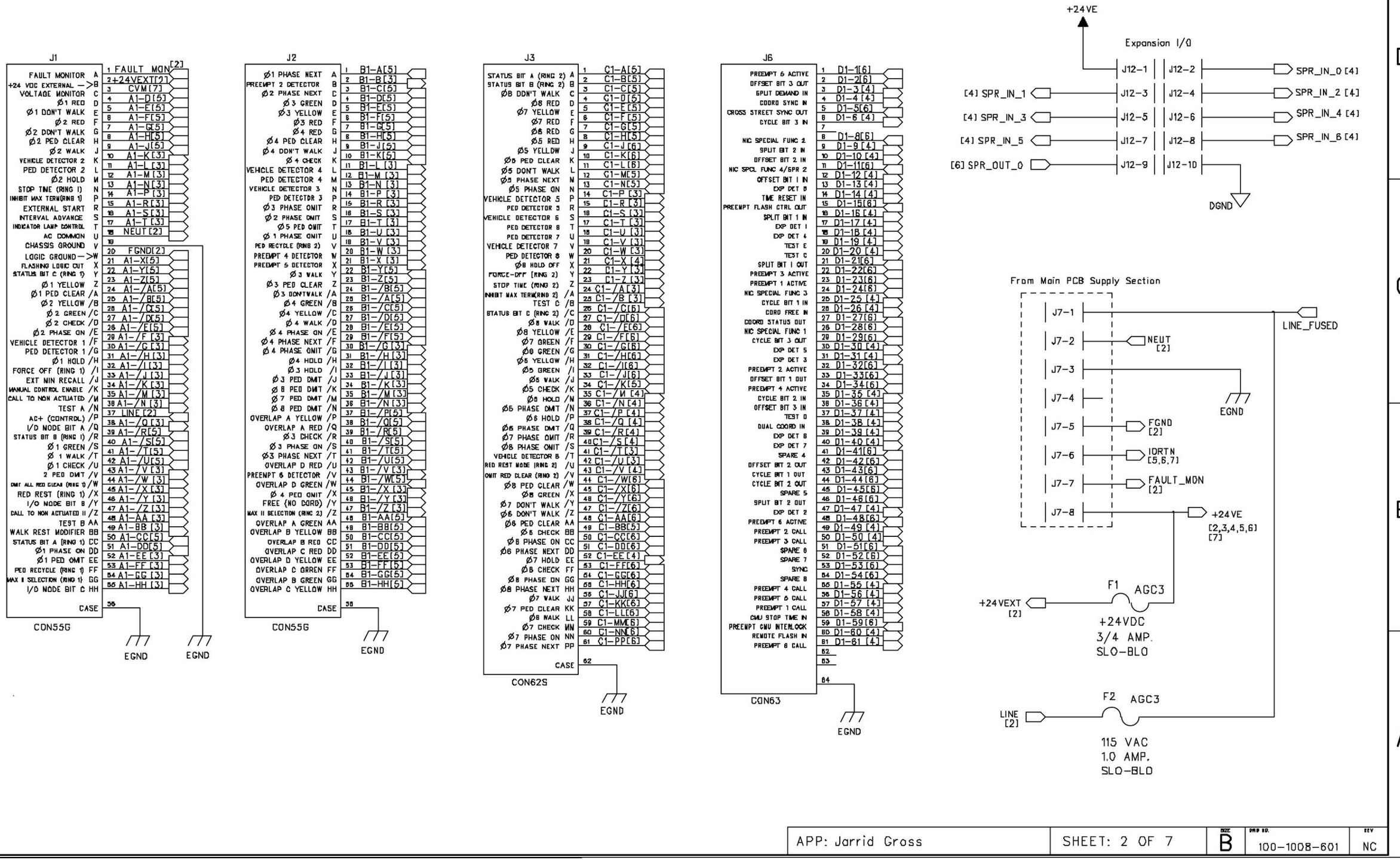
APP: JARRID GROSS	SHEET: 3 OF 3	SIZE B	DWG NO. 100-1006-601	REV A

REVISION RECORD			
LTR	DESCRIPTION	APPROVED:	DATE:
NC	INITIAL RELEASE ECO# 21200	JARRID GROSS	7/27/04

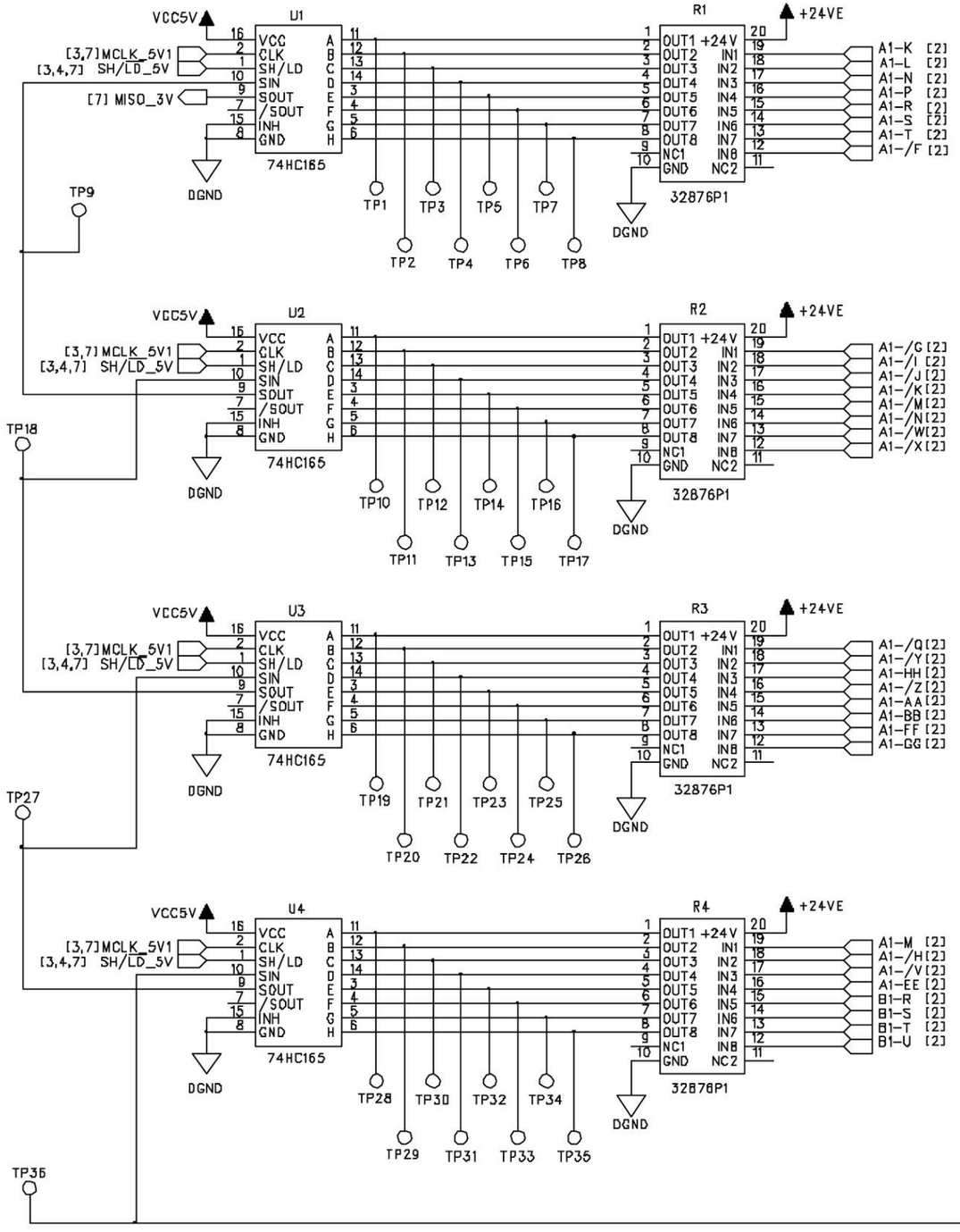
ECONOLITE CONTROL PRODUCTS INC

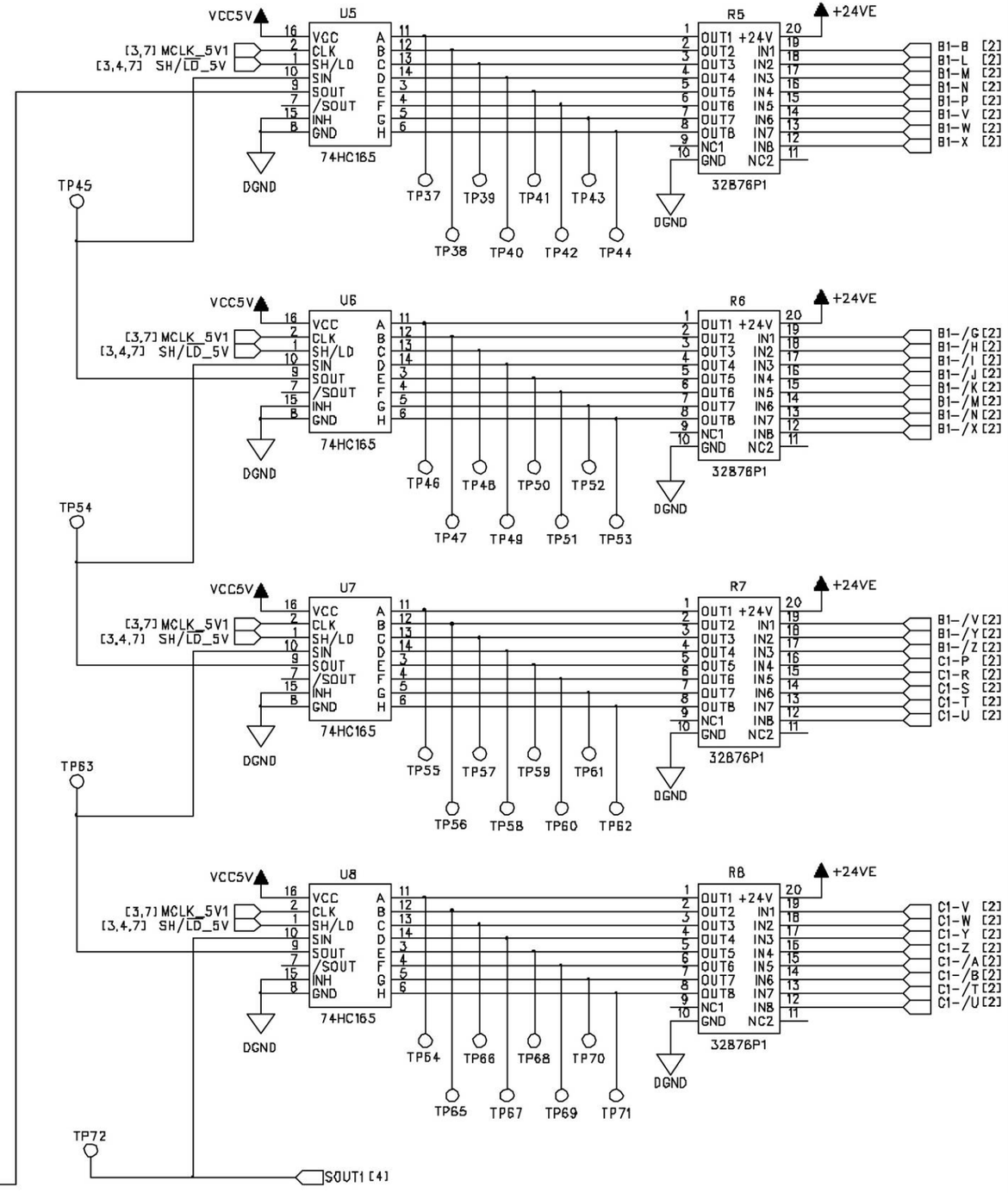
3360 E. LA PALMA AVE.
ANAHEIM, CALIFORNIA 92806

DR: Jarrid Gross	07-07-03	TITLE: SCHEMATIC ASC III TS2 TYPE 2 INTERFACE			
CHK: Jarrid Gross	07-16-04				
ENG: Jarrid Gross	07-16-04				
APP: Jarrid Gross	07-16-04	SHEET: 1 OF 7	SIZE: B	DWG NO: 100-1008-601	REV: NC

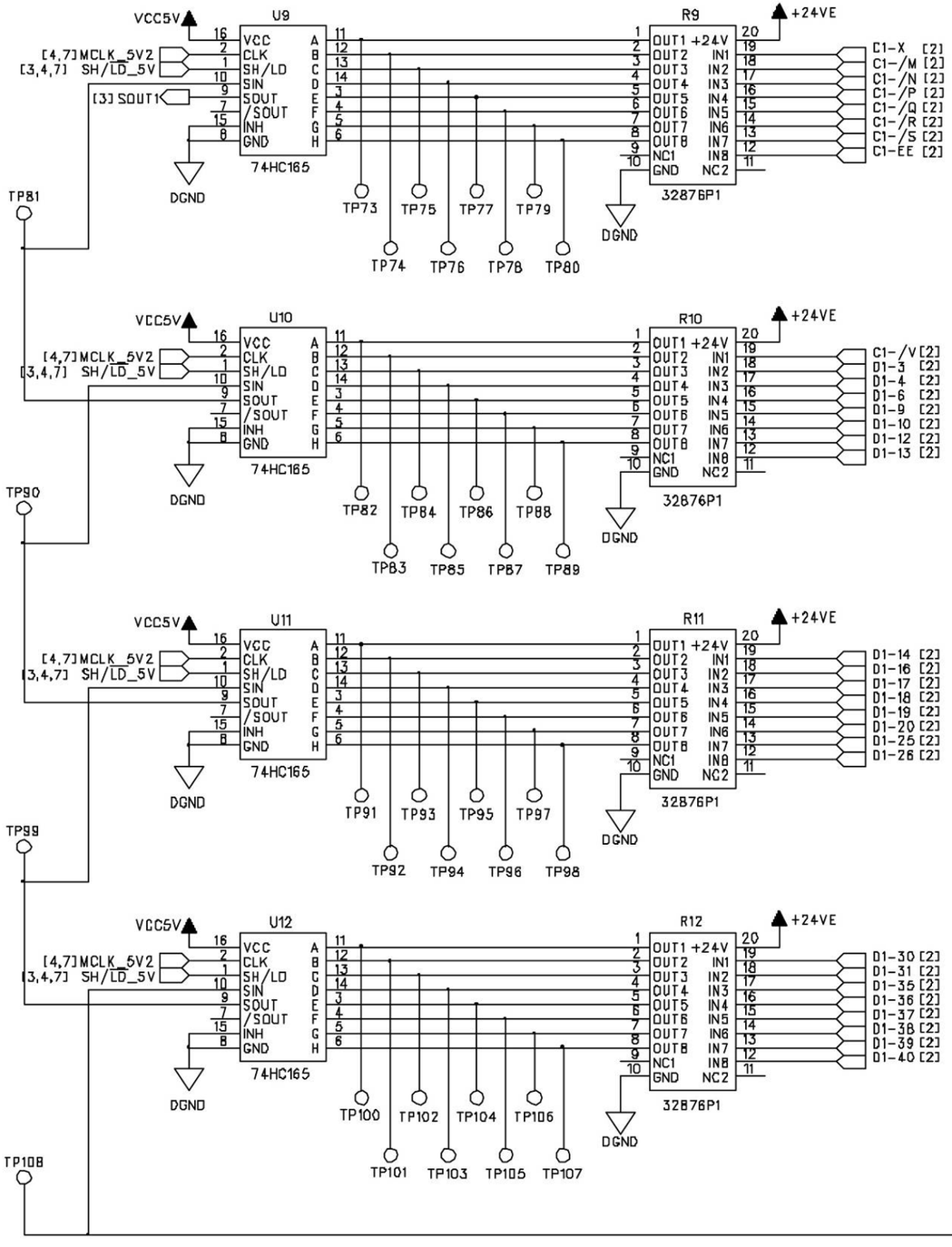


APP: Jarrid Gross	SHEET: 2 OF 7	SIZE B	DWG NO. 100-1008-601	REV NC

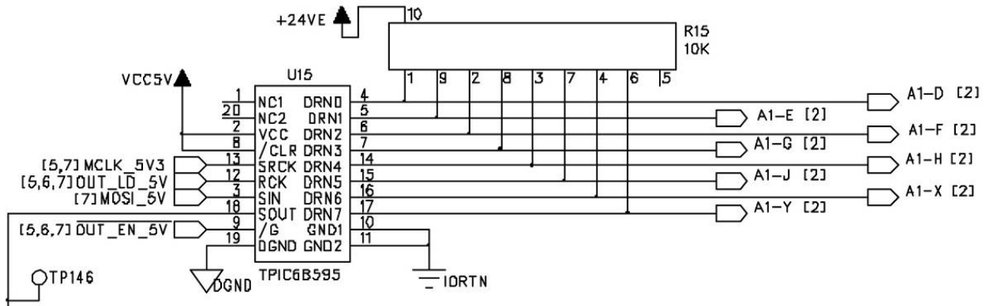


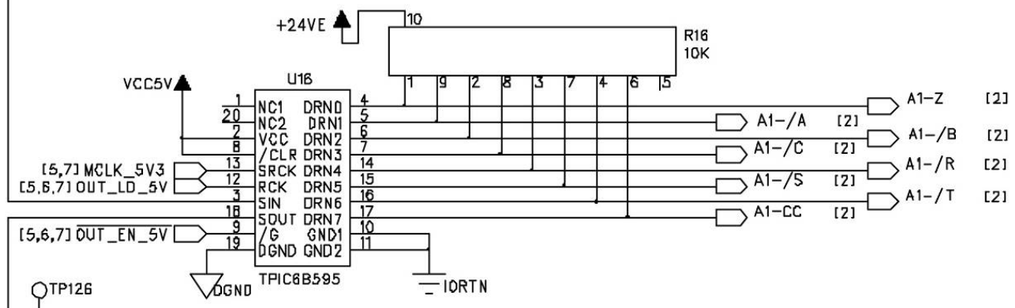


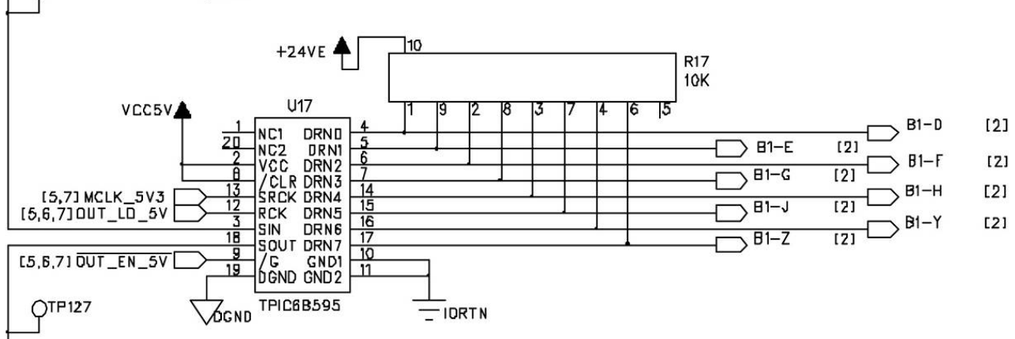
APP: JARRID GROSS	SHEET: 3 OF 7	SIZE B	DWG NO. 100-1008-601	REV NC

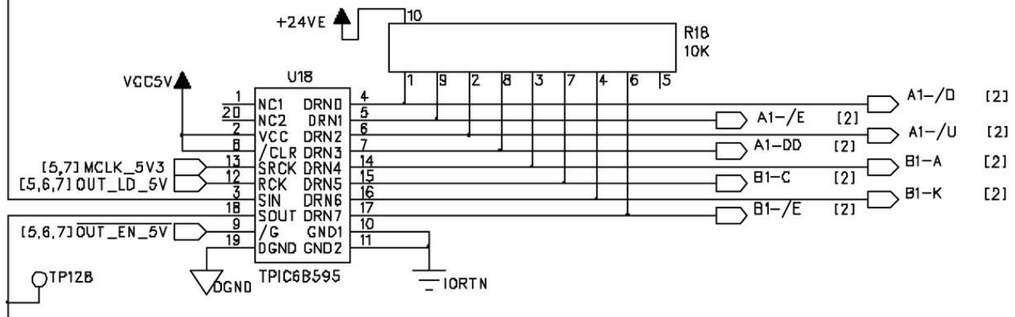


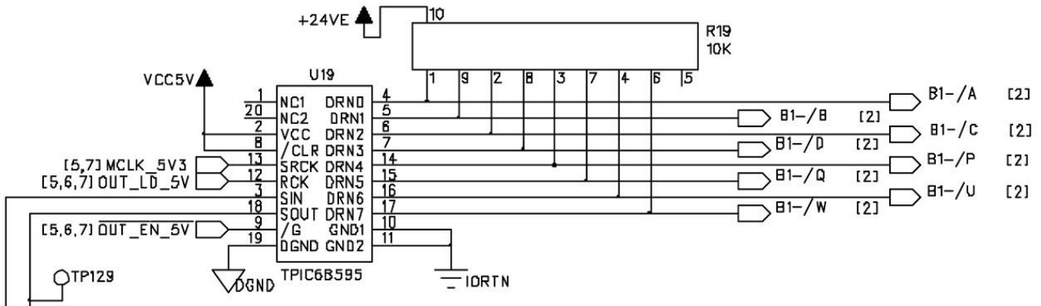
APP: JARRID GROSS		SHEET: 4 OF 7	SIZE B	DWG NO. 100-1008-601	REV NC

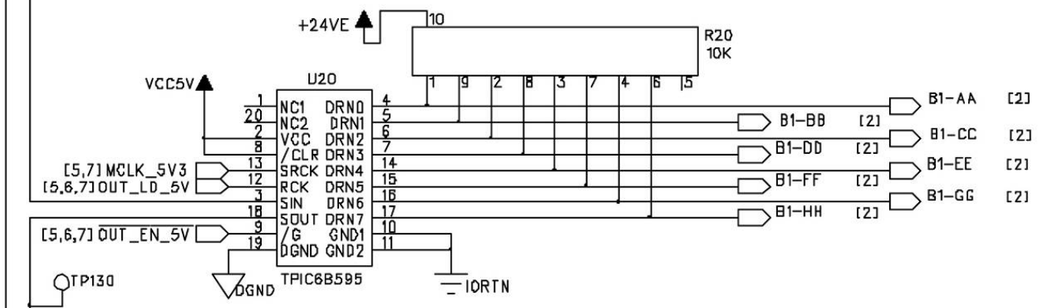


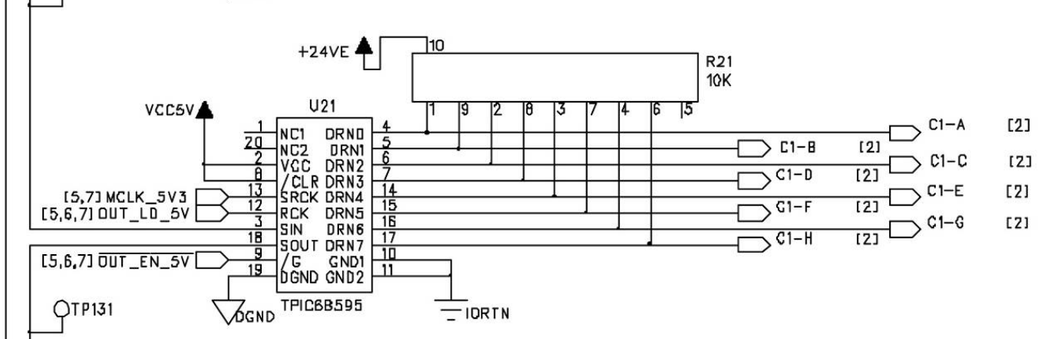


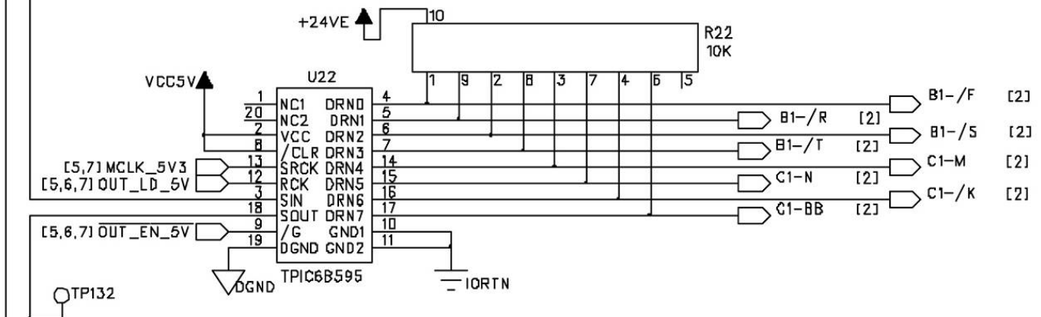




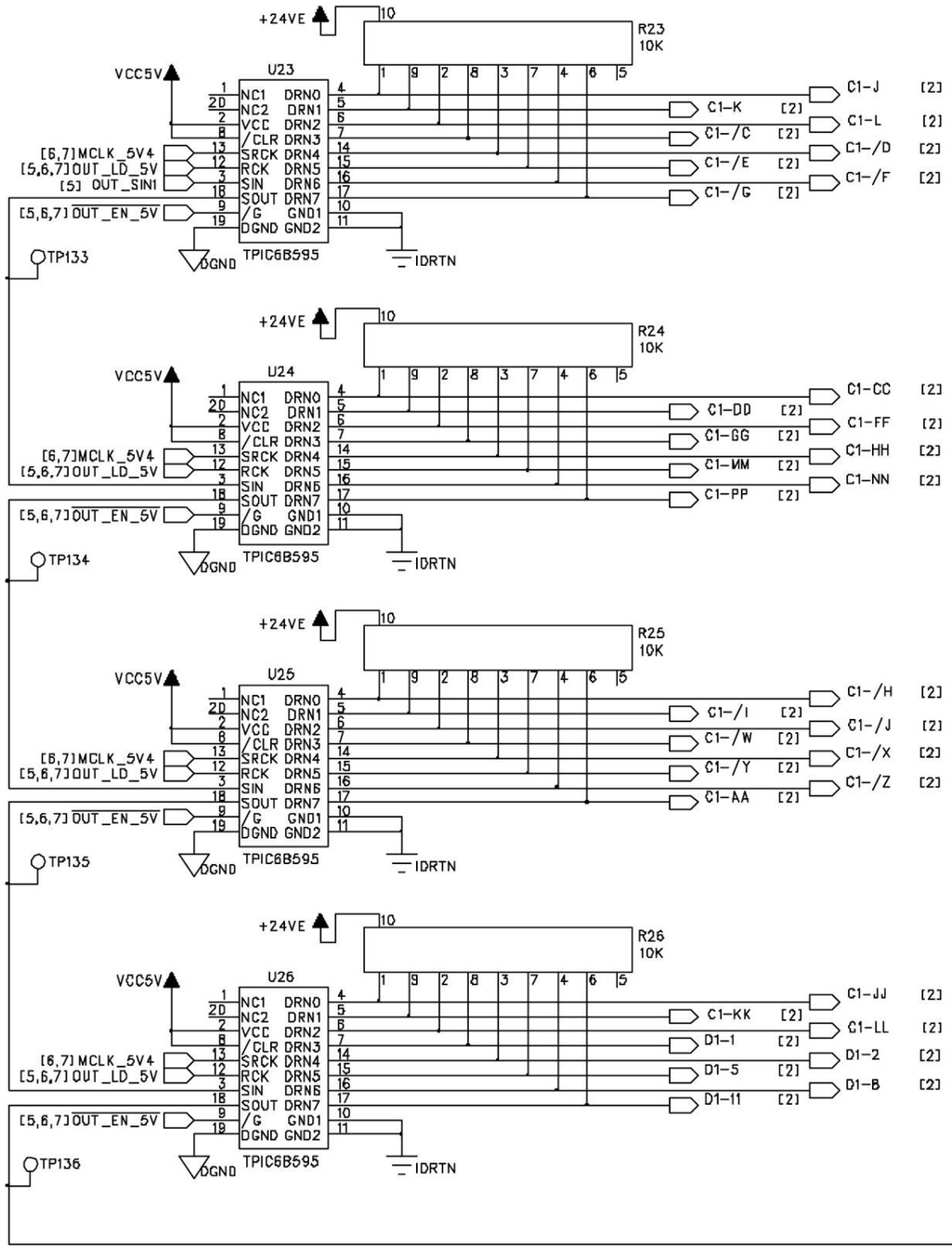


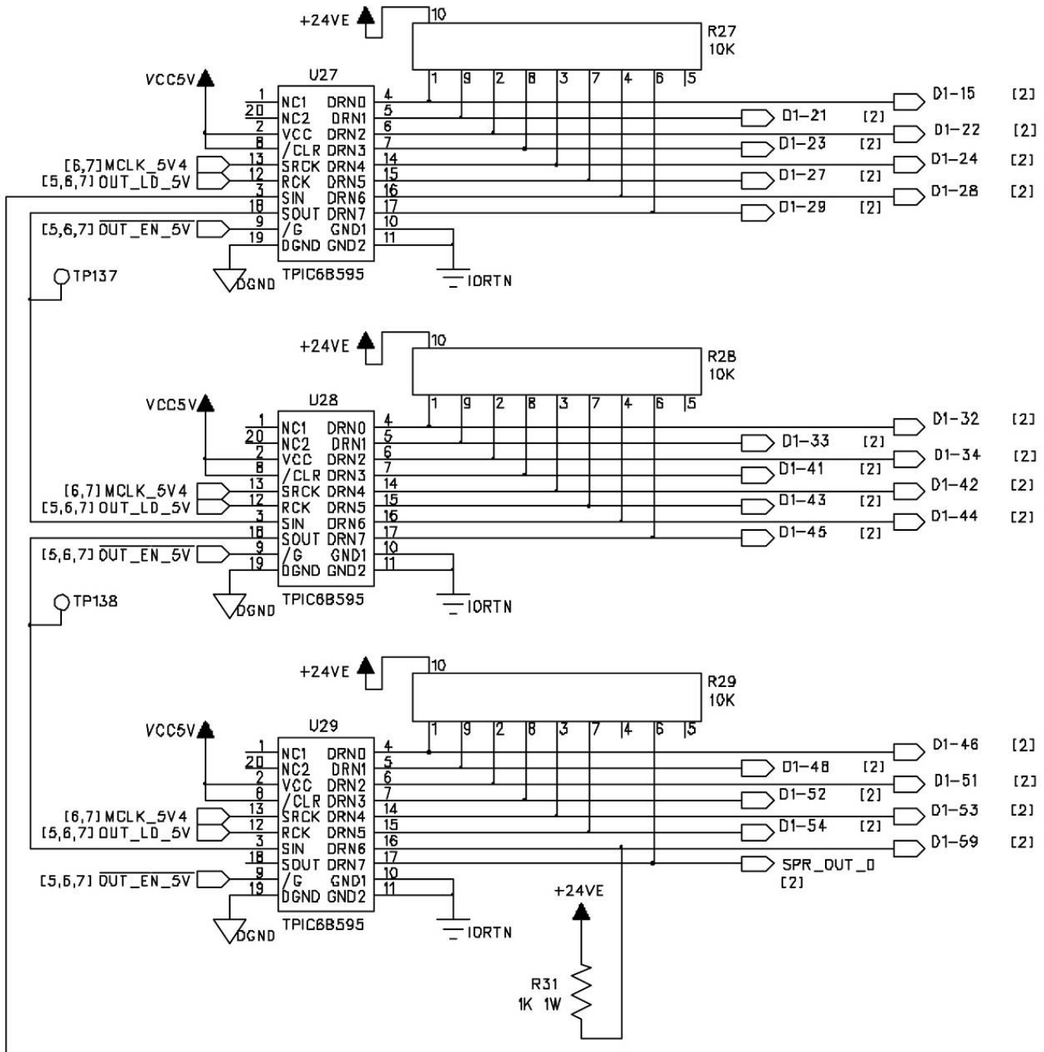






APP: JARRID GROSS		SHEET: 5 OF 7	SIZE B	DWG NO. 100-1008-601	REV NC





APP: JARRID GROSS		SHEET: 6 OF 7	SIZE B	DWG NO. 100-1008-601 / REV NC

5V Power Source

U30 — TPS60140

VCC3V, VCC5V, DGND, TP154

C1 .1uF
C2 100uF 10V
C3 10 uf 6.3V
C4 2.2 uf 10V
C5 2.2 uf 10V
C6 10 uf 10V
C7 100uF 10V
C8 .1uF

TP139, TP140, TP141, TP142

I/O PCB Interface

J8-1 … J8-12

R30 10K

MOSI_3V
MISO_3V
MCLK_3V
SH/LD_3V
OUT_LD_3V
OUT_EN_3V
CVM_OUT

MISO_3V [3]

U31-A — 74AHC244

MOSI_5V [5]
SH/LD_5V [3,4]
OUT_LD_5V [5,6]
OUT_EN_5V [5,6]

U31-B — 74AHC244

MCLK_5V1 [3]
MCLK_5V2 [4]
MCLK_5V3 [5]
MCLK_5V4 [6]

TP143, TP144, TP145, TP147, TP148, TP149, TP150, TP151, TP152, TP153

+24VE
10K R33
R32 2.49k
Q1 MMBT2222A
CR1 33V
CVM [2]
IORTN

C9 C10 C11 C12 C13 C14 C15 C16 .1uF
C17 C18 C19 C20 C21 C22 C23 C24 .1uF
C25 C26 C27 C28 C29 C30 C31 C32 .1uF
C33 C34 C35 C36 C37 C38 C39 C40 .1uF

Test Points

JP1 JP2 JP3 JP4 JP5 JP6

APP: JARRID GROSS		SHEET: 7 OF 7	SIZE B	DWG NO. 100-1008-601	REV NC

REVISION RECORD			
LTR	DESCRIPTION	APPROVED:	DATE:
NC	INITIAL RELEASE ECO#21601	Jarrid Gross	04-23-05

ECONOLITE CONTROL PRODUCTS INC
3360 E. LA PALMA AVE.
ANAHEIM, CALIFORNIA 92806

DR: Hasmukh Patel	02-29-04
CHK: M. CHU	08-01-05
ENG: Jarrid GROSS	04-23-05
APP: Gary Duncan	8/19/05

TITLE
SCHEMATIC,
ASC/3 TELEMETRY MAIN PCB

SHEET: 1 OF 6	SIZE B	DWG NO. 100-1032-601	REV NC

6 5 4 3 2 1

D C B A

[3] GPO3
[3] GPO2
[3] GPO1
[3] GPO0
[3] GPI15
[3] GPI14
[3] GPI13
[3] GPI12
[3] GPI11
[3] GPI10
[3] GPI9
[3] GPI8
[3] GPI7
[3] GPI6
[3] GPI5
[3] GPI4

10k R13

DGND

VCC3V

VCORE

GPI0 [3]
GPI1 [3]
GPI2 [3]
GPI3 [3]

VCC3V

10k R12

R32
33
*INSTALL FOR 25 PIN TELEM APP.

DGND

MODEM_TX [6]
MODEM_CTS [6]
MODEM_DCD [6]
CS_CODEC [4]
XMIT_ON [4]

MODEM_RX [6]
MODEM_RTS [6]
DAT_VALID [6]
FDUX/HDUX [4]

TP54 TP55 TP56 TP57

UB

TMS320VC5501

[6] EMU1
[6] EMU0
[6] TDO
[6] TDI
[6] TRST
[6] TCK
[6] TMS

Pin Connection Notes:

HPIENA low to disable
TIM0/1 low to prevent float
NMI pin has internal pullup
ECLKIN,EMIFCLKS is low to disable ECLKOUT1/2
HR/W,HCNTL0/1 low to prevent floating
HCS,HDS1,HDS2, high to prevent float
SCA,SCL I2C sigs low to prevent floating

I/O Configuration Notes:

A[21:18] are PGPIO[3:0] set as telem inputs
A[2:17] are allowed to float per datasheet
D[27:16] are PGPIO[15:4] set as telem inputs
D[31:28] are PGPIO[19:16] set as telem outputs
D[15:0] are allowed to float per datasheet
C[15:0] are PGPIO[35:20] set as outputs for current reduction
HD[7:0] are PGPIO[43:36] set as outputs for current reduction
HC[1:0] are PGPIO[45:44] set as outputs for current reduction

GPIO Strapping Notes:

GPIO7 must be pulled low at reset so UART gets muxed pins
GPIO6 must be pulled low to enable PGPIOs
GPIO4 determines the oscilator type, If high, EXT osc is used.
GPIO2:0 are for the boot mode (001=spi,111=ASYNC)
GPIO[7:0] Strapping is (00X1X001)

Remove R5 for Async Bootstrap

VCC3V VCC3V

C34 .1uF

U9 LM8364

R3 4.99k

C62 DNI .1uF

DGND

reset ee-prog JP3

VCC3V

R14 10k

HOST_RX [2,6]
HOST_TX [2,6]

TP30 TP31 TP32

VCC3V VCC3V

C36 .1uF

U7 AT25F512

[2] CS_EE
[2] MISO

MCLK [2,4]
MOSI [2,4]

DNI R6 0 R5 DNI R4

CS_EE [2]

R31 33

TP21 TP23 TP25 TP27 TP29
TP20 TP22 TP24 TP26 TP28

HOST_RX [2,6]
HOST_TX [2,6]
FSX1 [4]
CLKRX1 [4]
DX1 [4]
FSR1 [4]
DR1 [4]

DX0 MOSI [2,4]
CLKX0 MCLK [2,4]
DR0 MISO [2]

TP33

DSP_CLK [4]

VCC3V

C35 .1uF

18.432 mhz

U10 System/CPU Clock

R7 33

TP19

APP: Jarrid Gross	SHEET: 2 OF 6	SIZE B	DWG NO. 100-1032-601	REV NC

25 Pin I/O Connector

DSP GPIO Pins

Inputs

Outputs

+24VI

32876P1

[6] SYS_DET_C2
[6] TLM_SPARE_1
[6] SYS_DET_A2
[6] EXT_ADDR_EN
[6] SYS_DET_A1
[6] MAINT_REQ
[6] SYS_DET_C1
[6] ALARM_1

R10

DGND

TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10

VCC5V

VCC3V

C15 .1uF

C16 .1uF

U12
74LVC4245A

TP34 TP35 TP36 TP37 TP38 TP39 TP40 TP41

GPI0 [2]
GPI1 [2]
GPI2 [2]
GPI3 [2]
GPI4 [2]
GPI5 [2]
GPI6 [2]
GPI7 [2]

[6] SYS_DET_B1
[6] LOCAL_FLASH
[6] TLM_SPARE_2
[6] SYS_DET_B2
[6] SYS_DET_D1
[6] CONFLICT_FLASH
[6] SYS_DET_D2
[6] ALARM_2

R11

C17 .1uF

C18 .1uF

U13
74LVC4245A

TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18

TP42 TP43 TP44 TP45 TP46 TP47 TP48 TP49

GPI8 [2]
GPI9 [2]
GPI10 [2]
GPI11 [2]
GPI12 [2]
GPI13 [2]
GPI14 [2]
GPI15 [2]

10k R16

[6] SPC_FUNC_1
[6] SPC_FUNC_2
[6] SPC_FUNC_3
[6] SPC_FUNC_4

U14
ULN2003AD

TP50 TP51 TP52 TP53

GPO0 [2]
GPO1 [2]
GPO2 [2]
GPO3 [2]

APP: Jarrid Gross		SHEET: 3 OF 6	SIZE B	DWG NO. 100-1032-601	REV NC

3v Levels

5v Levels

Hasmukh, note irregular pinout on SW1!
Hasmukh, Look into if R29,R30 can be smaller package!

SPI CONTROL
[2] CS_CODEC
[2] MOSI
[2] MCLK

MCBSP INTERFACE
[2] CLKRX1
[2] DX1
[2] FSX1
[2] DR1
[2] FSR1
[2] DSP_CLK

U2
TLV320AIC23B
BVDD, CLKOUT, BCLK, DIN, LRCIN, DOUT, LRCOUT, HPVDD, LHPOUT, RHPOUT, HPGND, LOUT, ROUT, AVDD
DGND, DVDD, XTO, XTI/MCLK, SCLK, SDIN, MODE, CS, LLINEIN, RLINEIN, MICIN, MICBIAS, VMID, AGND

VCC3V, VCC3V
TP58, TP62
R17 33
C22 .33uF
R21 4.99k
3V3_MIDPT [4]
DGND, AGND, DGND

TP60, TP59
C21 DNI
C26 .33uF

Anti Alias 30khz @-3db
TP80, TP79, TP63
C59 1500pf
U17-B TLV2472
R28 16.9k
R27 2.15k
U17-A TLV2472
TP81, C58 220pf
VCC2V5
C24 470pf
TP64
R26 11.8k

VCC5V
D4 BAT54S
DGND

L1
V18ZA3 RV2
RX- [6]
RX+ [6]
R29 10 BWH

Duplex Switch
Half Full
SW1
FDUX/HDUX [2]
DGND

124khz @-3db, A= -1.532
R20 16.9k
XMIT_ON [2]
R18 6.04k
R19 4.99k
TP65
TLV2470 U16
TP66
R25 120

L2
V18ZA3 RV1
TX- [6]
TX+ [6]
R30 10 BWH

TP82, TP67
C23 470pf
VCC2V5

VCC5V
D5 BAT54S
DGND

3V3_MIDPT [4]
TP61
C20 .1uF
C19 2.2 uf 10V
AGND

VCC3V
U2.1 C27 .1uF
U2.8 C28 .1uF
U2.27 C29 .1uF
DGND

VCC3V
U2.13 C30 .1uF
AGND

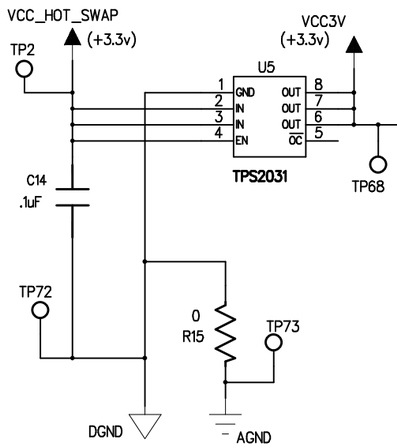
VCC5V
U16 C31 .1uF
AGND

VCC5V
U17 C60 .1uF
AGND

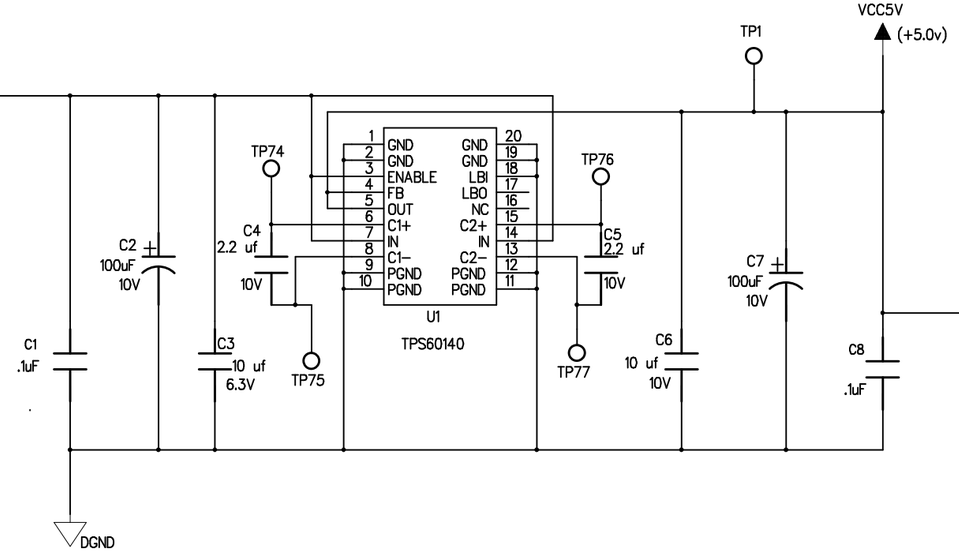
With a Codec output of 2.85vpp (.864 FS), Vo is 4.366vpp, drive = +6dbm
With a Codec output of 2.02vpp (.612 FS), Vo is 3.095vpp, drive = +3dbm
With a Codec output of 1.43vpp (.433 FS), Vo is 2.191vpp, drive = 0dbm

APP: Jarrid Gross	SHEET: 4 OF 6	SIZE B	DWG NO. 100-1032-601	REV NC

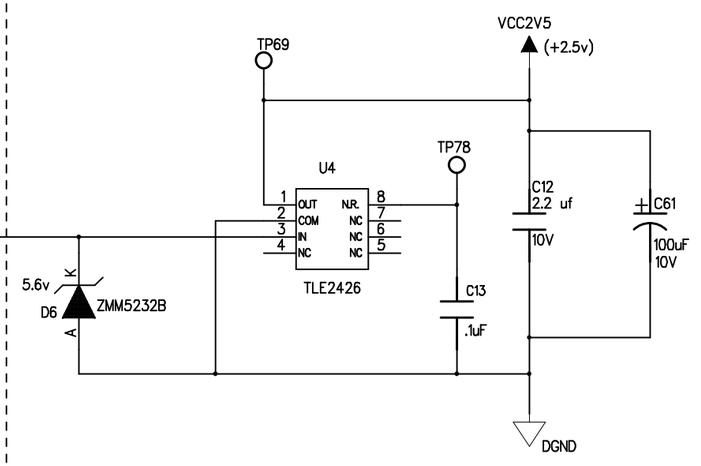
Hot Swap Circuit



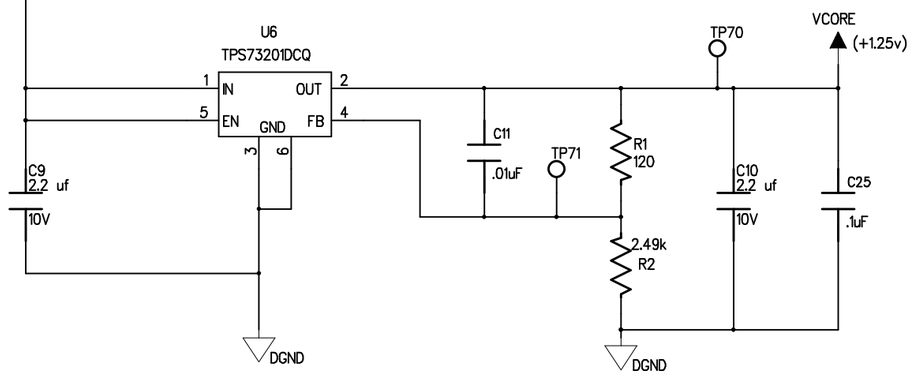
5V Power Source



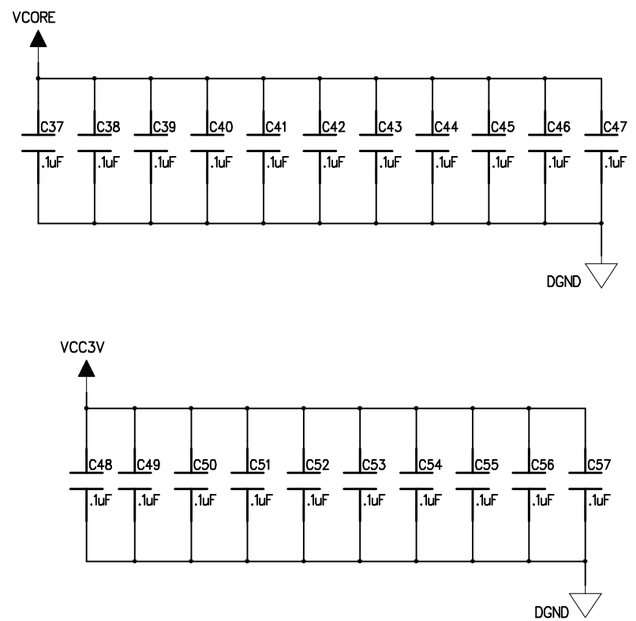
Analog Virtual Ground



Core Power Source

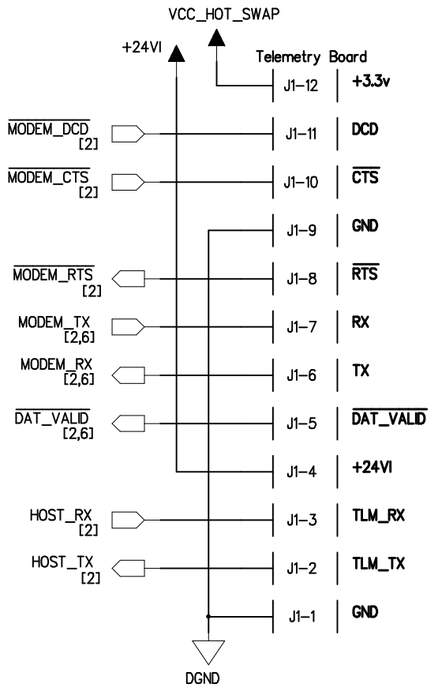


U8 Decoupling

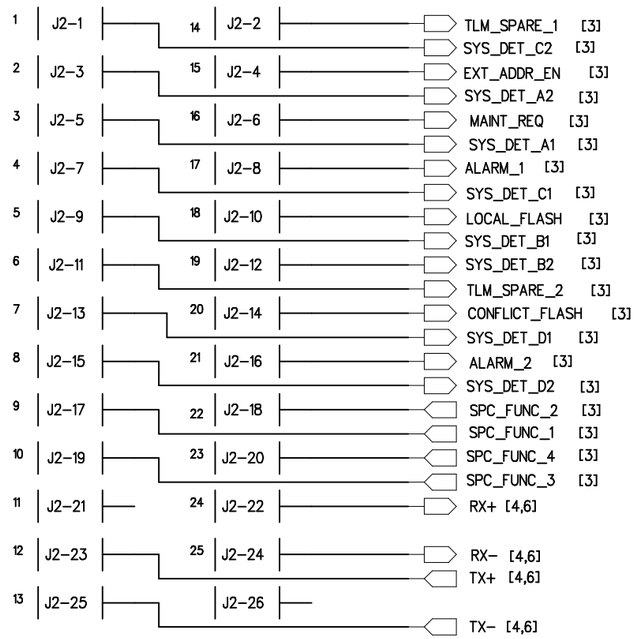


APP: Jarrid Gross	SHEET: 5 OF 6	SIZE B	DWG NO. 100-1032-601	REV NC

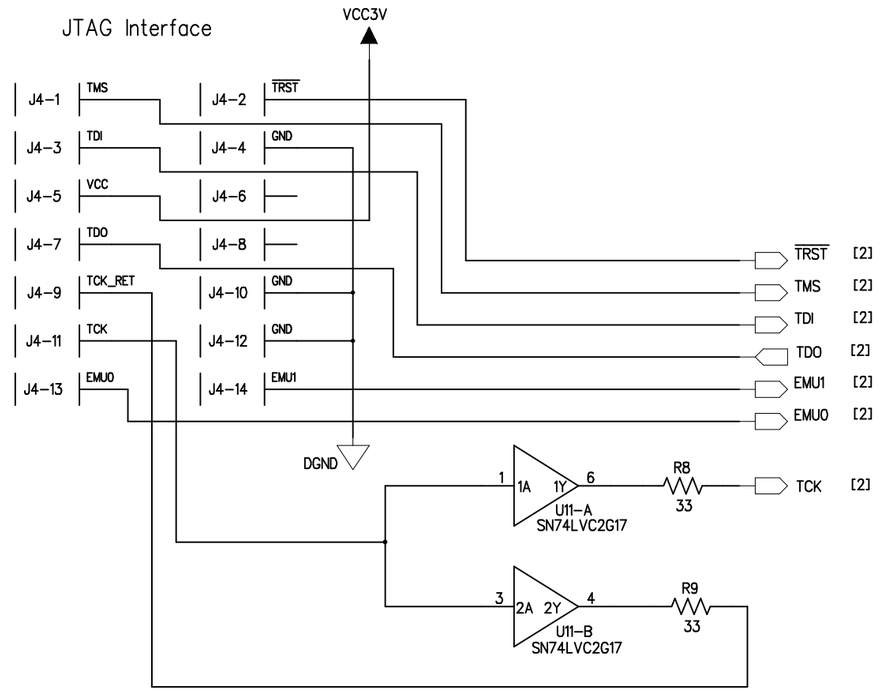
Host Interface Connector



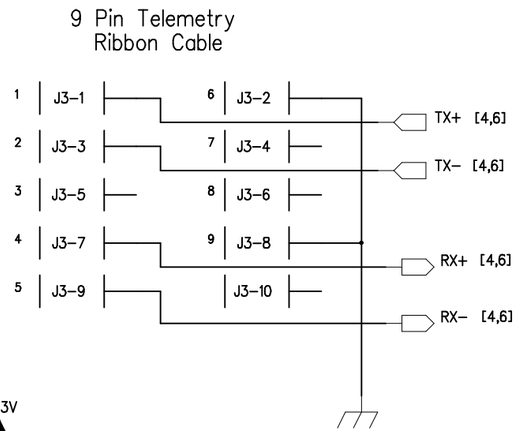
25 Pin Telemetry Ribbon Cable

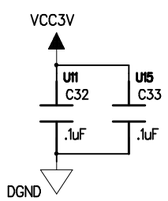


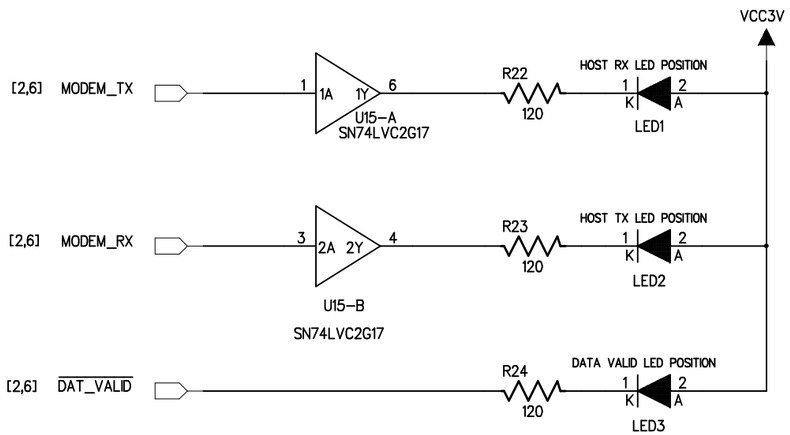
JTAG Interface

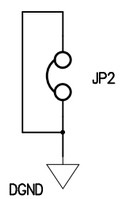


9 Pin Telemetry Ribbon Cable





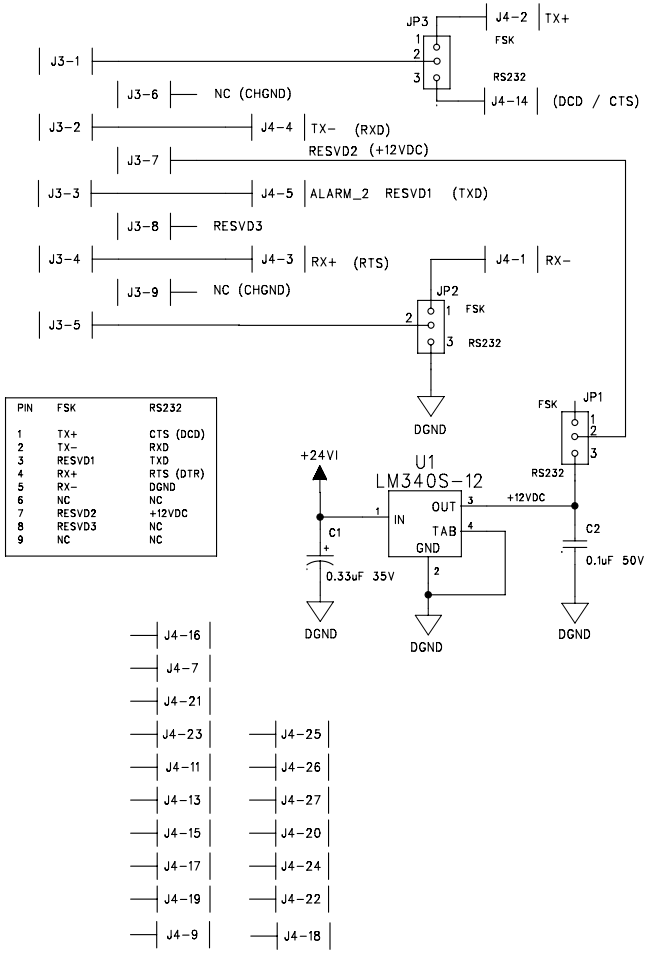




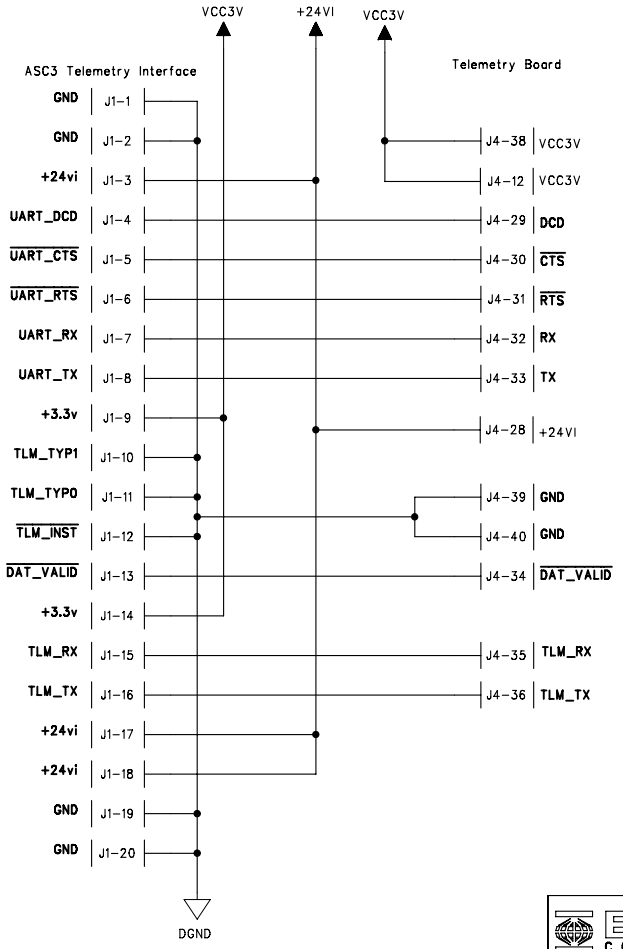
APP: Jarrid Gross	SHEET: 6 OF 6	SIZE B	DWG NO. 100-1032-601	REV NC

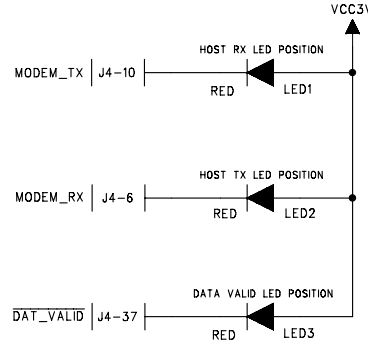
REVISION RECORD				
LTR	DESCRIPTION	ECO NO.	APPROVED:	DATE:
NC	INTIAL RELEASE	22368	J. ROSE	04-26-07

9 Pin DB CONNECTOR



PIN	FSK	RS232
1	TX+	CTS (DCD)
2	TX-	RXD
3	RESVD1	TXD
4	RX+	RTS (DTR)
5	RX-	DGND
6	NC	NC
7	RESVD2	+12VDC
8	RESVD3	NC
9	NC	NC





ECONOLITE CONTROL PRODUCTS INC
3360 E. LA PALMA AVE.
ANAHEIM, CALIFORNIA 92806

DRW:	S. LUU	04-23-07
CHK:	J. SHIELD	04-23-07
ENG:	J. ROSE	04-23-07
APP:	G. DUNCAN	04-24-07

TITLE: SCH, TELEMETRY CONN 9DB

SHEET: 1 OF 1 | SIZE: B | DWG NO.: 100-1091-601 | REV: NC

REVISION RECORD				
LTR	DESCRIPTION	ECO NO.	APPROVED:	DATE:
NC	INTIAL RELEASE	22368	J. ROSE	04-26-07

DB-25 CONNECTOR — **2mm Board to Board Connector**

J2-1	J4-24	SYS_DET_C2
J2-14	J4-23	TLM_SPARE_1
J2-2	J4-25	SYS_DET_A2
J2-15	J4-26	EXT_ADDR_EN
J2-3	J4-27	SYS_DET_A1
J2-16	J4-21	MAINT_REQ
J2-4	J4-22	SYS_DET_C1
J2-17	J4-20	ALARM_1
J2-5	J4-19	SYS_DET_B1
J2-18	J4-18	LOCAL_FLASH
J2-6	J4-17	TLM_SPARE_2
J2-19	J4-16	SYS_DET_B2
J2-7	J4-15	SYS_DET_D1
J2-20	J4-14	CONFLICT_FLASH
J2-8	J4-13	SYS_DET_D2
J2-21	J4-5	ALARM_2
J2-9	J4-11	SPC_FUNC_1
J2-22	J4-9	SPC_FUNC_2
J2-10	J4-8	SPC_FUNC_3
J2-23	J4-7	SPC_FUNC_4
J2-11	J4-3	RX+
J2-24	JP2	FSK / RS232
J2-12	J4-2	TX+
J2-25	J4-1	RX-
J2-13		

JP2: 1 = FSK, 2 = DGND, 3 = RS232

PIN	FSK	RS232
12	TX+	TXD
13	TX-	+12VDC
24	RX+	GND
25	RX-	RXD

20-Pin Molex Connector — **2mm Board to Board Connector**

GND	J1-1		
GND	J1-2		
+24vi	J1-3		
UART_DCD	J1-4	J4-29	DCD
UART_CTS	J1-5	J4-30	CTS
UART_RTS	J1-6	J4-31	RTS
UART_RX	J1-7	J4-32	RX
UART_TX	J1-8	J4-33	TX
+3.3v	J1-9		
TLM_TYP1	J1-10		
TLM_TYP0	J1-11	J4-39	GND
TLM_INST	J1-12	J4-40	GND
DAT_VALID	J1-13	J4-34	DAT_VALID
+3.3v	J1-14		
TLM_RX	J1-15	J4-35	TLM_RX
TLM_TX	J1-16	J4-36	TLM_TX
+24vi	J1-17		
+24vi	J1-18		
GND	J1-19		
GND	J1-20		

VCC3V, +24VI, VCC3V; J4-38 VCC3V, J4-12 VCC3V, J4-28 +24VI; DGND

U1 LM340S-12: 1 = IN, 2 = GND, 3 = OUT, 4 = TAB

C1 0.33uF 35V; C2 0.01uF 50V; DGND

J4-4 TX-; JP1: 1 = FSK, 2 = RS232

VCC3V

MODEM_TX | J4-10 — HOST RX LED POSITION — RED — LED1

MODEM_RX | J4-6 — HOST TX LED POSITION — RED — LED2

DAT_VALID | J4-37 — DATA VALID LED POSITION — RED — LED3

ECONOLITE CONTROL PRODUCTS INC
3360 E. LA PALMA AVE.
ANAHEIM, CALIFORNIA 92806

DRW:	S. LUU	04-23-07
CHK:	J. SHIELD	04-23-07
ENG:	J. ROSE	04-23-07
APP:	G. DUNCAN	04-24-07

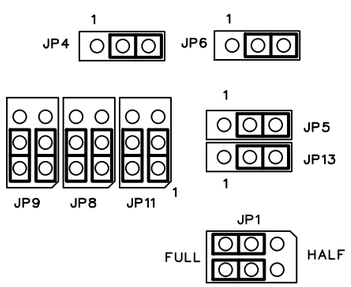
TITLE: SCH, TELEMETRY CONN 25DB

SHEET: 1 OF 1 | SIZE: B | DWG NO.: 100-1092-601 | REV: NC

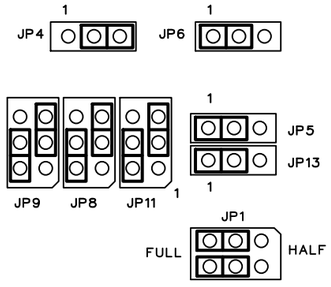
REVISION RECORD				
LTR	DESCRIPTION	ECO NO.	APPROVED:	DATE:
NC	INTIAL RELEASE	22368	J. ROSE	04-26-07
A	SEE ECO	22628	J. ROSE	12-05-07
B	SEE ECO	22851	J. ROSE	05-06-08

Main Board
Jumper Configurations

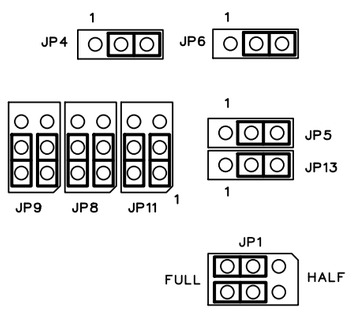
FSK 25-Pin



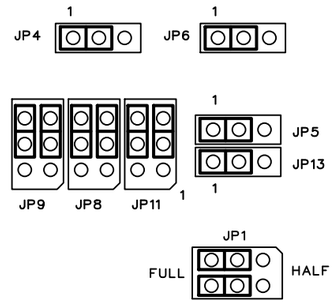
RS-232 25-Pin



FSK 9-Pin



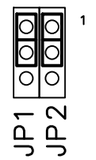
RS-232 9-Pin



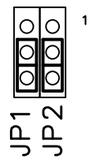
Daughter Board
Jumper Configurations

25-Pin Connector Board
Jumper Configurations

FSK

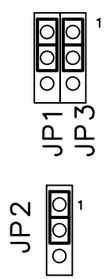


RS232

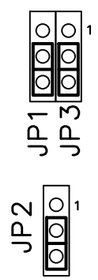


9-Pin Connector Board
Jumper Configurations

FSK



RS232

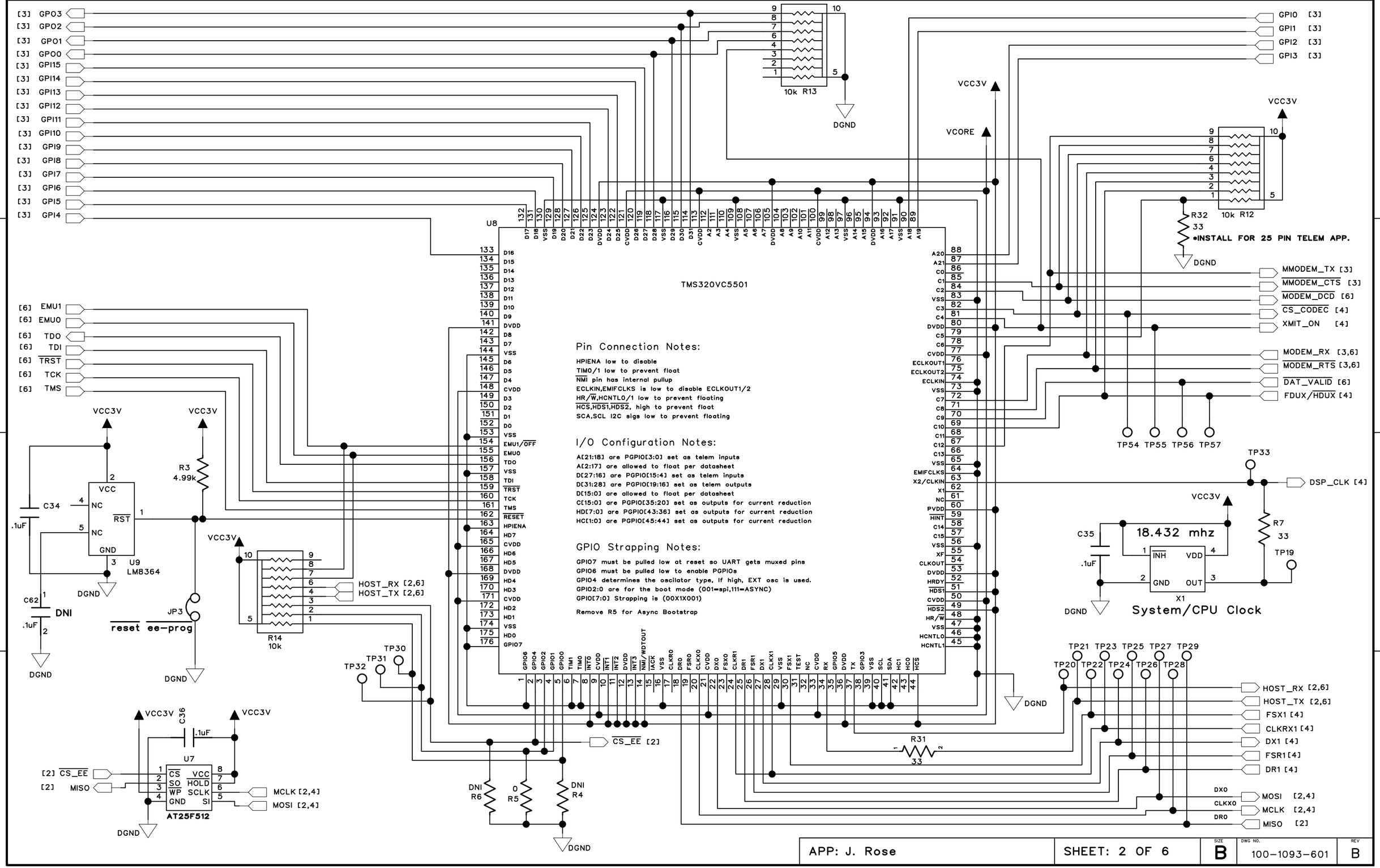


ECONOLITE
3360 E. LA PALMA AVE.
ANAHEIM, CALIFORNIA 92806

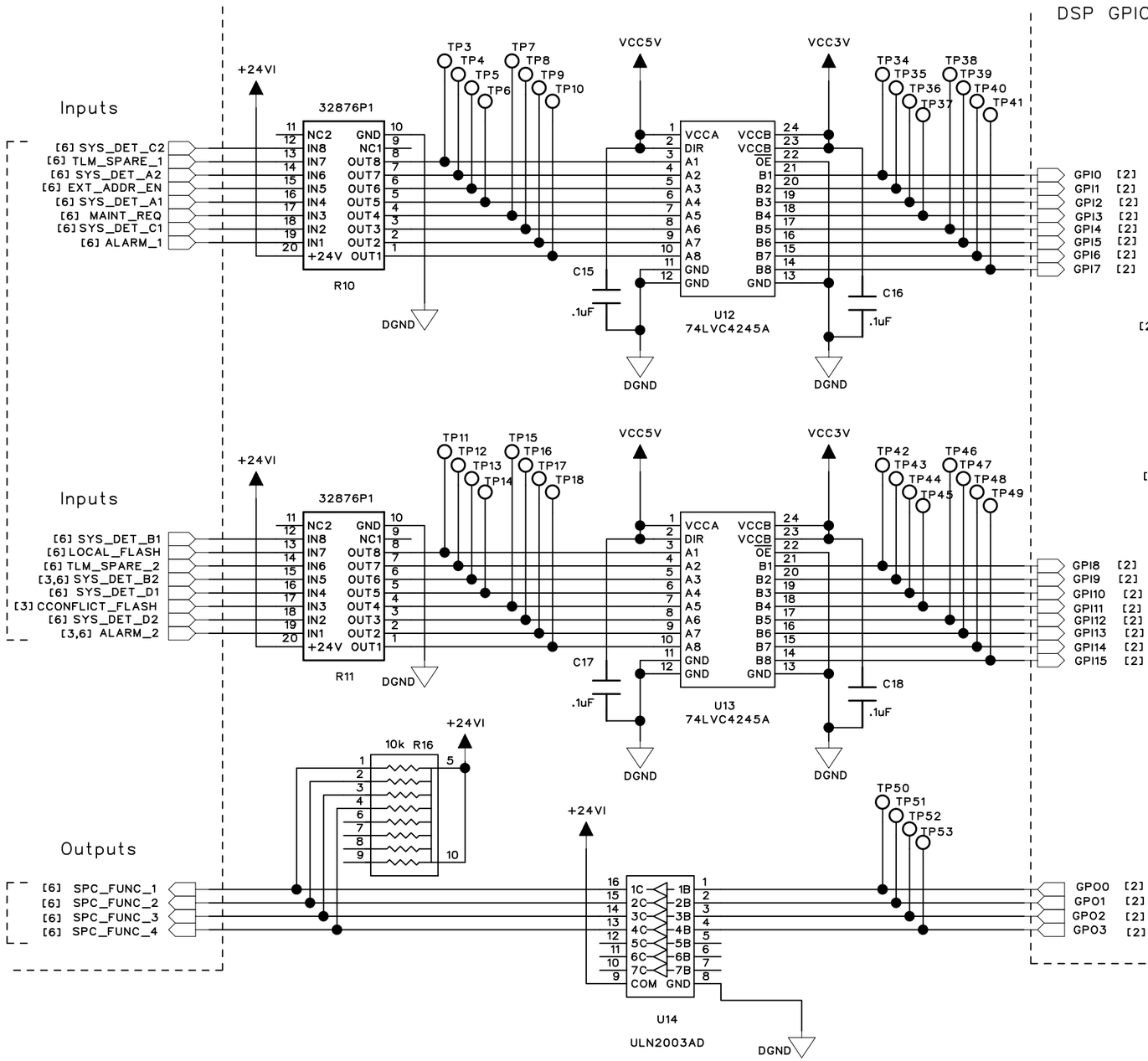
DRW:	S. LUU	04-23-07
CHK:	J. SHIELD	04-23-07
ENG:	J. ROSE	04-23-07
APP:	G. DUNCAN	04-24-07

TITLE: SCHEMATIC,
ASC/3 TELEMETRY MAIN PCB

SHEET: 1 OF 6 | SIZE: B | DWG NO.: 100-1093-601 | REV: B



APP: J. Rose	SHEET: 2 OF 6	SIZE B	DWG NO. 100-1093-601	REV B



APP: J. Rose		SHEET: 3 OF 6	SIZE B	DWG NO. 100-1093-601	REV B

6 5 4 3 2 1

D C B A

3v Levels

5v Levels

SPI CONTROL
[2] CS_CODEC
[2] MOSI
[2] MCLK

MCBSP INTERFACE
[2] CLKRX1
[2] DX1
[2] FSX1
[2] DR1
[2] FSR1

[2] DSP_CLK

VCC3V
VCC3V
R17 33
TP58
U2
TLV320AIC23B
BVDD 1
CLKOUT 2
BCLK 3
DIN 4
LRCIN 5
DOUT 6
LRCOUT 7
HPVDD 8
LHPOUT 9
RHPOUT 10
HPGND 11
LOUT 12
ROUT 13
AVDD 14
DGND 28
DVDD 27
XTO 26
XTI/MCLK 25
SCLK 24
SDIN 23
MODE 22
CS 21
LLINEIN 20
RLINEIN 19
MICIN 18
MICBIAS 17
VMID 16
AGND 15
DGND
AGND
DGND
TP62
R21 4.99k
3V3_MIDPT [4]
C22 .33uF

Anti Alias 30khz @-3db
TP80
TP79
TP63
C59 1500pf
U17-B TLV2472
R28 16.9k
R27 2.15k
U17-A TLV2472
R26 11.8k
TP81
C58 220pf
VCC2V5
C24 470pf
TP64
VCC5V
D4 BAT54S
DGND
L1
RRX- [3]
RV2
RX+ [6]
R29 10 BWH

Duplex Jumper
Half Full
Full Duplex Shown
JP1
FDUX/HDUX [2]
DGND

124khz @-3db, A= -1.532
R20 16.9k
XMIT_ON [2]
TP60
TP59
DNI C21
C26 .33uF
R18 6.04k
R19 4.99k
TLV2470 U16
TP65
TP66
R25 120
TP82
TP67
C23 470pf
VCC2V5
L2
TTX- [3]
RV1
TTX+ [3]
R30 10 BWH

VCC5V
D5 BAT54S
DGND

With a Codec output of 2.85vpp (.864 FS), Vo is 4.366vpp, drive = +6dbm
With a Codec output of 2.02vpp (.612 FS), Vo is 3.095vpp, drive = +3dbm
With a Codec output of 1.43vpp (.433 FS), Vo is 2.191vpp, drive = 0dbm

VCC3V
U2.1 C27 .1uF
U2.8 C28 .1uF
U2.27 C29 .1uF
DGND

VCC3V
U2.13 C30 .1uF
AGND

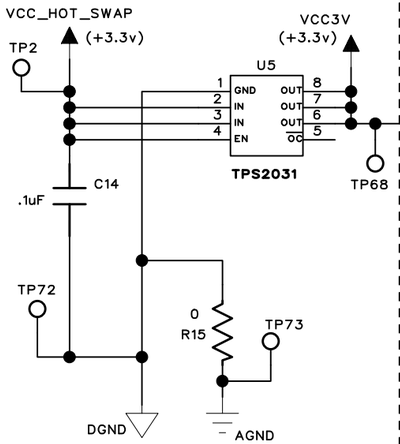
VCC5V
U16 C31 .1uF
AGND

VCC5V
U17 C60 .1uF
AGND

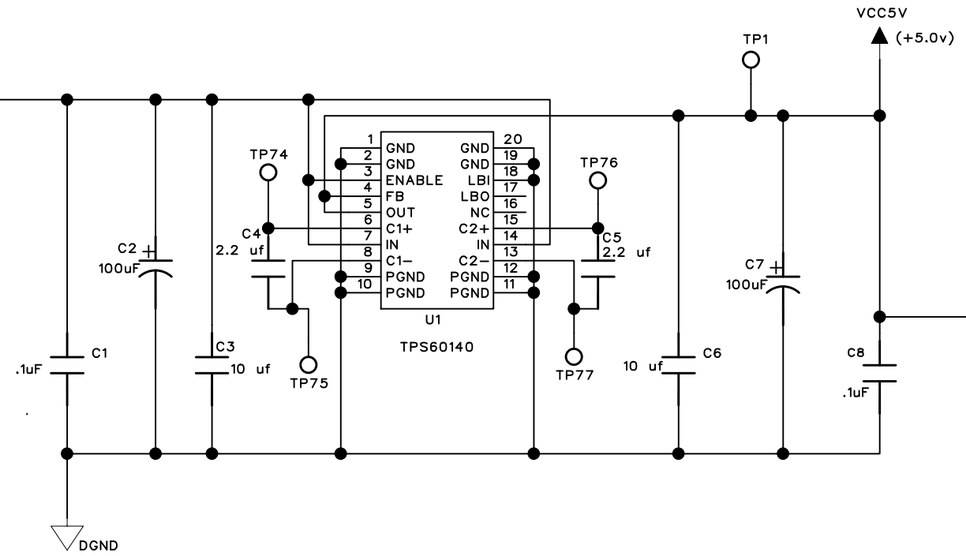
3V3_MIDPT [4]
TP61
C20 .1uF
C19 2.2 uf
AGND

APP: J. Rose	SHEET: 4 OF 6	SIZE B	DWG NO. 100-1093-601	REV B

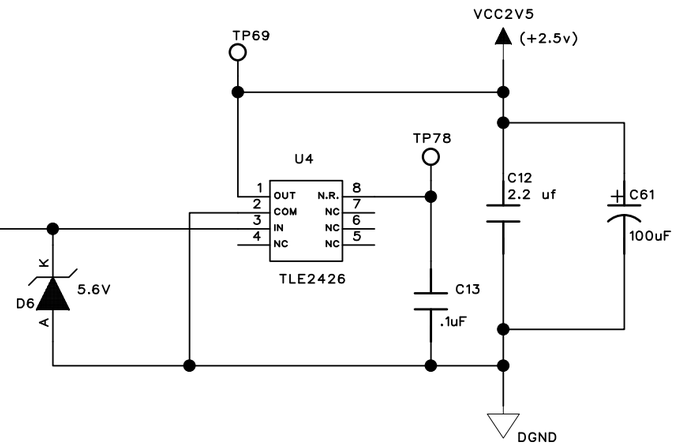
Hot Swap Circuit



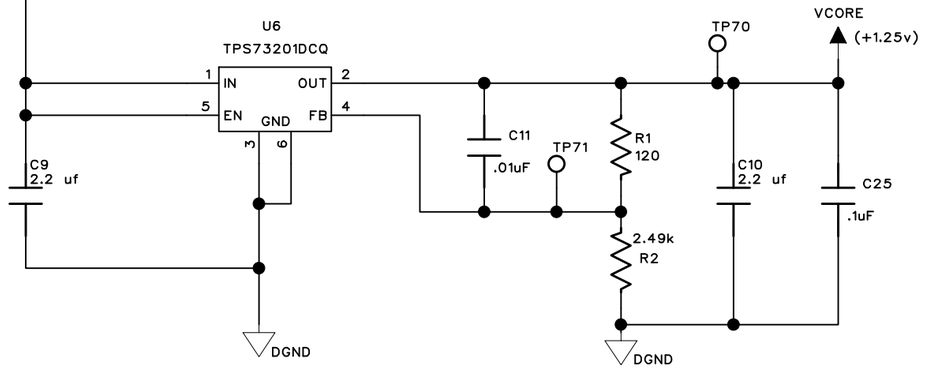
5V Power Source



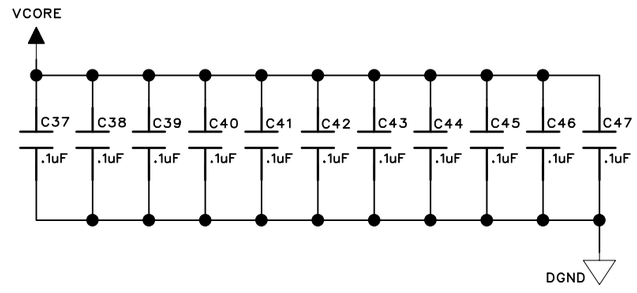
Analog Virtual Ground

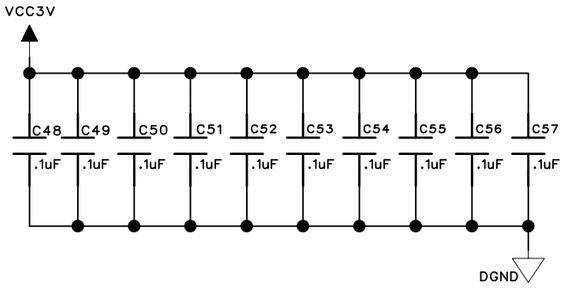


Core Power Source



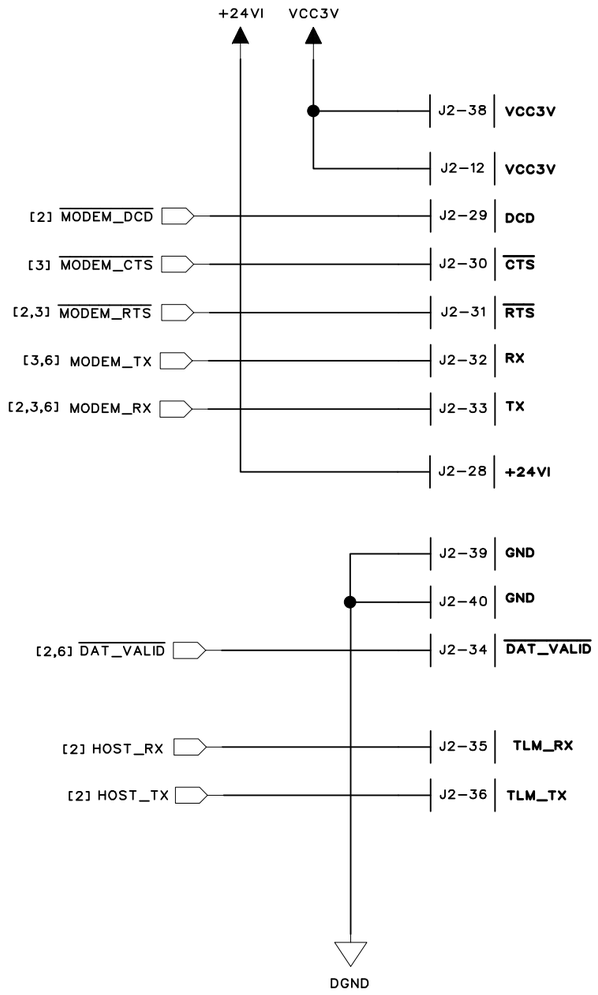
U8 Decoupling

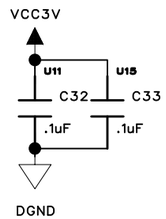




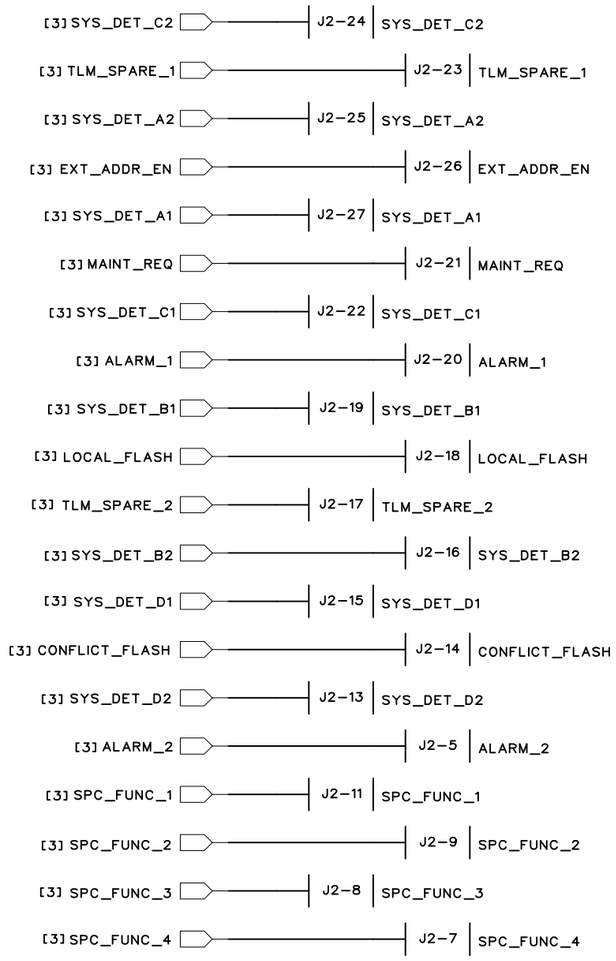
APP: J. Rose	SHEET: 5 OF 6	SIZE B	DWG NO. 100-1093-601	REV B

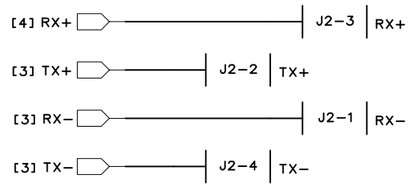
From Host Interface connector



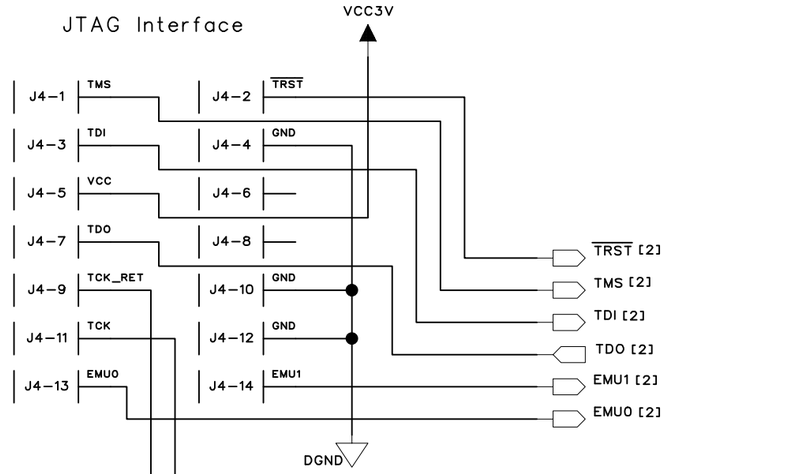


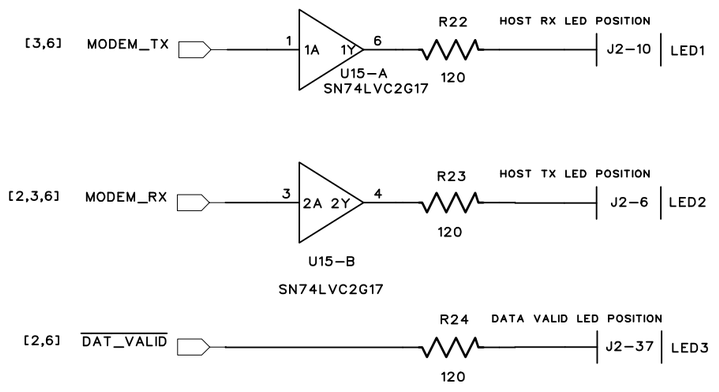
FROM 25 Pin and 9 Pin DB CONNECTOR

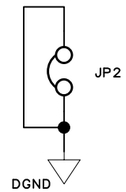




JTAG Interface

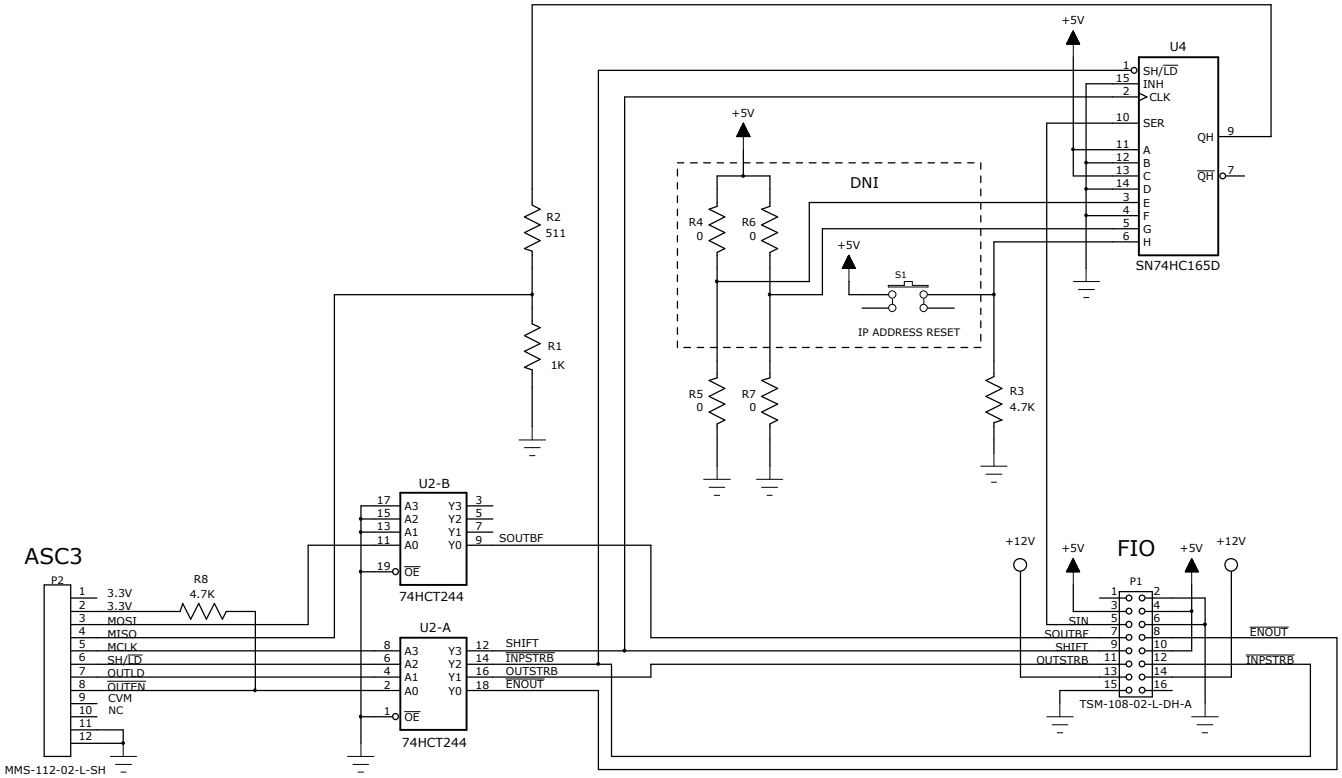


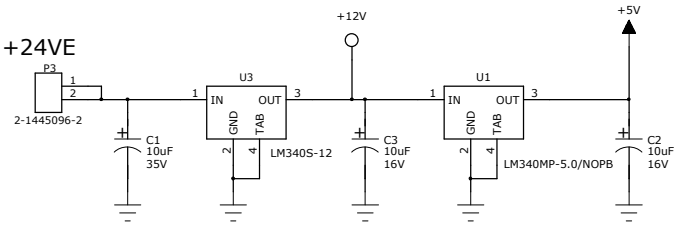




APP: J. Rose	SHEET: 6 OF 6	SIZE B	DWG NO. 100-1093-601	REV B

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:
NC	ECO# 22829	J. ROSE	05-13-08
A	ECO# 22995	J. ROSE	





DRAWN: J. SHIELD	DATE: 08-21-07		
CHECKED: J. ROSE	DATED: 04-23-08		
ENGINEER: J. SHIELD	DATED: 04-23-08		
TEST ENGINEER: A. ISSAC	DATED: 04-23-08		
APPROVED: J. ROSE	DATED: 04-23-08		

ECONOLITE
3360 EAST LA PALMA AVENUE
ANAHEIM, CALIFORNIA 92806-2856

TITLE: ASC3RM FIELD I/O INTERFACE BOARD

CODE:	SIZE:	DRAWING NO:	REV:
	B	100-1119-601	A

SCALE: 1:1 SHEET: 1 OF 1

7. APPENDIX B: ASSEMBLY DRAWINGS

Appendix Contents

ASC/3 Unit Assembly (Drawing 100-0000-501, -502, -510, -511, Sheets 1-3)

Front Panel Assembly (Drawing 100-1030-501and -502, Sheets 1-2)

Ethernet Module Assembly (Drawing 100-1006-501)

Data Module Kit Assembly (Drawing 100-1007-501)

Assy, PCB, Telemetry, Main, ASC/3 (Drawing 100-1032-5xx, Sheets 1-2)

Assy, ASC/3, Telemetry Module (Drawing 100-1084-5xx, Sheets 1-3)

TS2-1 Power Cable Assembly (Drawing 100-1020-501)

TS2-2 Cable Assembly (Drawing 100-1019-501)

ASC/3 TS2 Type 2 I/F assembly (Drawing 100-1008-501)

Assy, PCB, FIO Interface, ASC/3 (Drawing 100-119-501)

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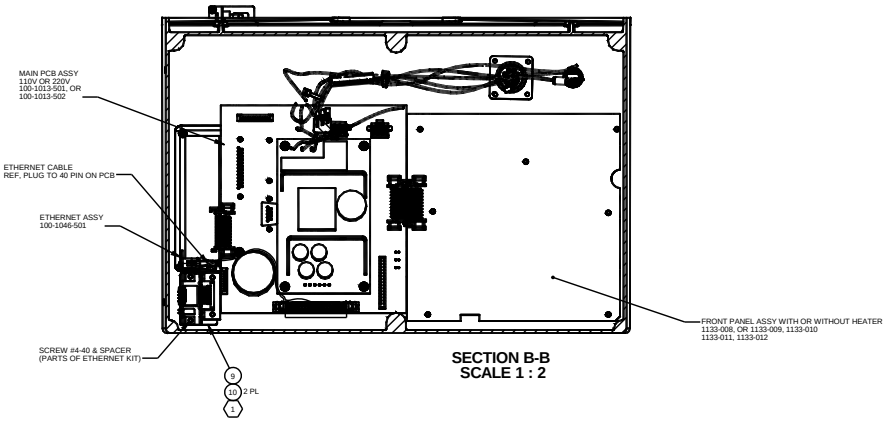
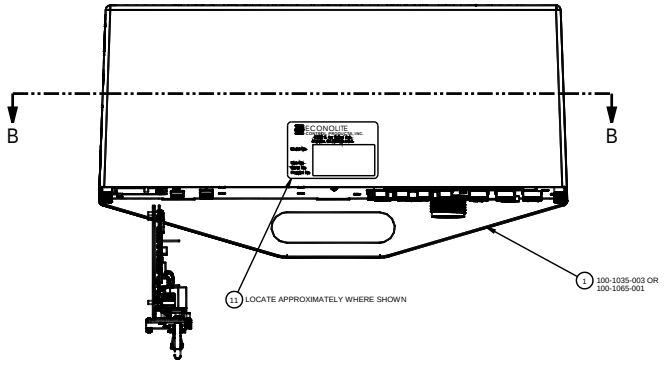
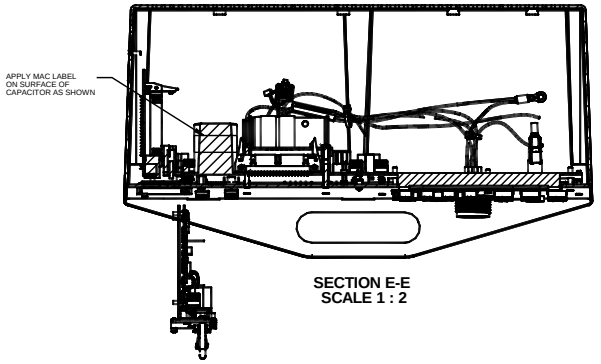
REVISIONS				
REV.	BY	E.C.O. NUMBER	DATE	APPROVED
NC	MC	21271	9-8-04	J.G.
A	MC	21359	11-30-04	J.G.
B	MC	21401	1-5-05	J.G.
C	MC	21445	2-23-05	J.G.
D	MC	21467	4-15-05	J.G.
E	RM	SEE ECO 22169	9-29-06	J.R.
F	MC	SEE ECO 22398	5-31-07	J.R.
G	MC	SEE ECO 22601	11-20-07	J.R.
H	RM	SEE ECO 22629	5-13-08	J.R.

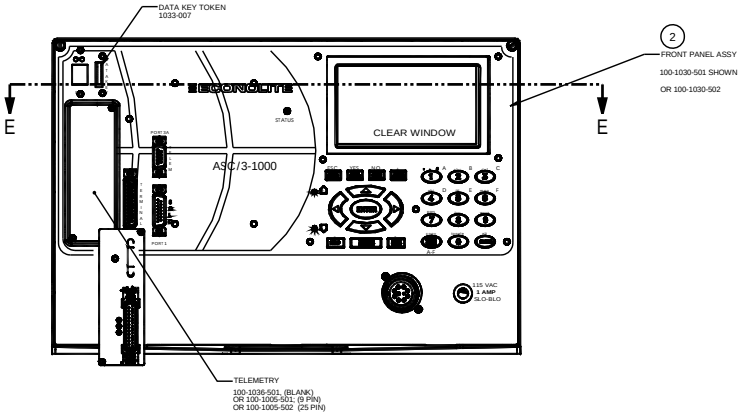


SECTION B-B
SCALE 1 : 2





SECTION E-E
SCALE 1 : 2



SEE CONFIGURATION BOM FOR COMPLETE LIST OF PARTS
EXAMPLE: ASC3110100000

DASH#	DESCRIPTION
511	ASSY, ASC/3-2100, TS2 TYPE 2 RACKMOUNT
510	ASSY, ASC/3-1000, TS2 TYPE 1 RACKMOUNT
509	ASSY, ASC/3-2100, TS2 TYPE 2 (SHEETMETAL)
508	ASSY, ASC/3-1000, TS2 TYPE 1 (SHEETMETAL)
502	ASSY, ASC/3-2100, TS2 TYPE 2 (CAST)
501	ASSY, ASC/3-1000, TS2 TYPE 1 (CAST)

(1) DISCARD ITEM 9, (COVER) WHEN ETHERNET ASSY IS APPLIED.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCE ON ALL MACHINED EDGES
PART MUST BE FREE OF ANY FOREIGN CONTAMINANTS
TOLERANCE:
DECIMAL: XX ± .03, XXX ± .010
ANGULAR: ± 0°30'

DRAWN: M. CHU 7-9-04
ENGR: M. CHU 7-9-04
CHK'D: G. ROS 7-9-04
APVD/QA: J. GROSS 8-24-04
MFG/PROD: E. RAAMOT 9-1-04
MATERIAL:
FINISH:

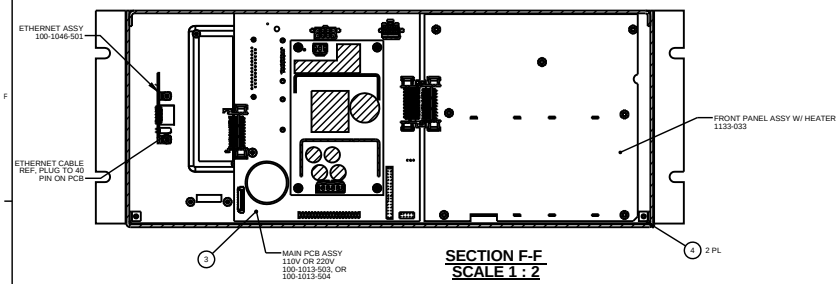
ECONOLITE CONTROL PRODUCTS, INC.
1360 E. Ist PALMA, ANAHEIM, CA. 92806

TITLE: UNIT ASSY, ASC/3

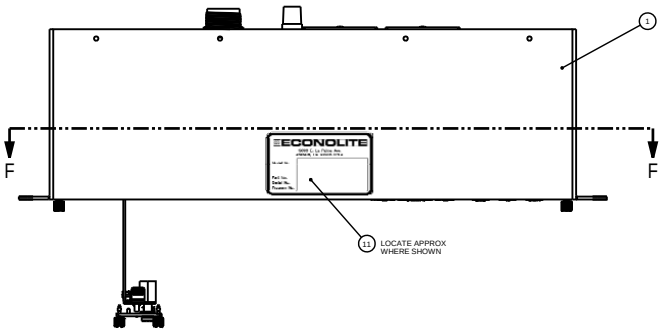
SIZE: D | CAGE CODE: 0FEW7 | DRAWING NO.: 100-0000-5XX | REV.: H
SCALE: 1:2 | CAD FILE: 100-0000-5XX.SLDDRW | Sheet 1 OF 3

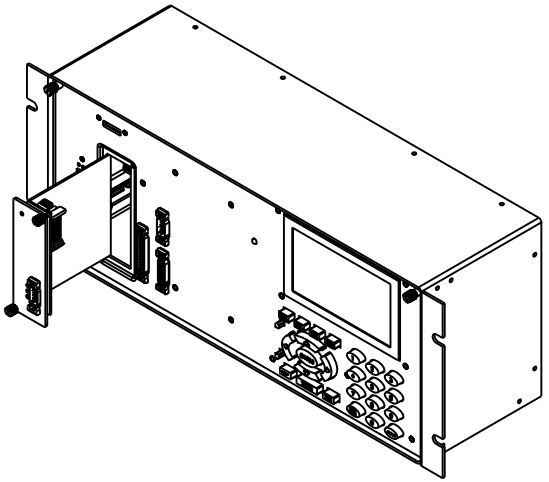
MODEL FILE: unitassy_514R4.SLDPRT

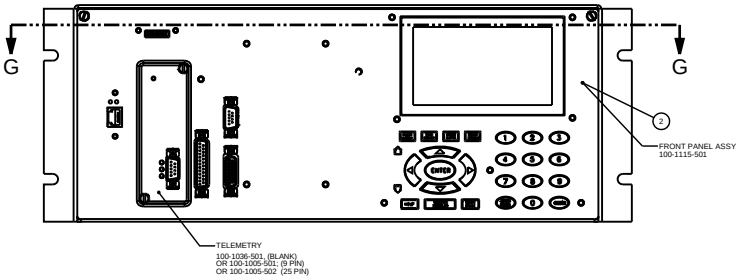
DO NOT SCALE DRAWING

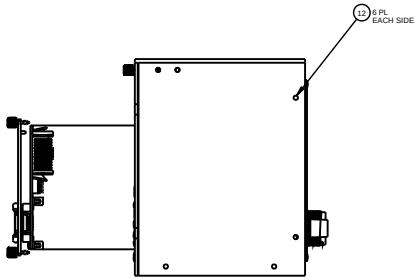


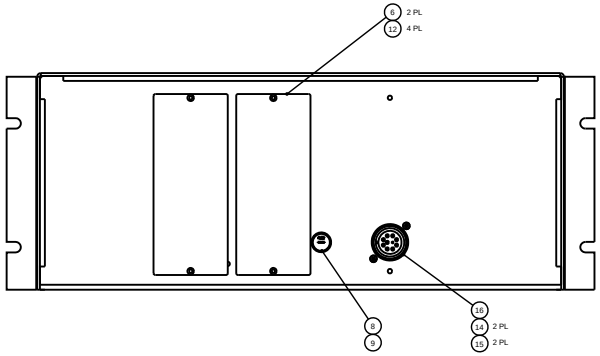
SECTION F-F
SCALE 1 : 2

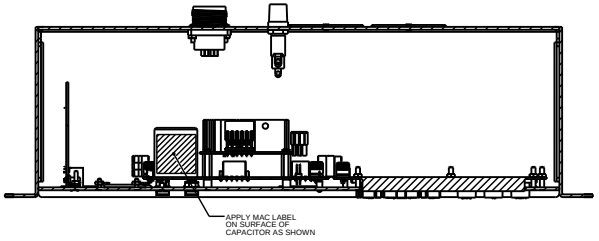












SECTION G-G
SCALE 1 : 2

510 SHOWN

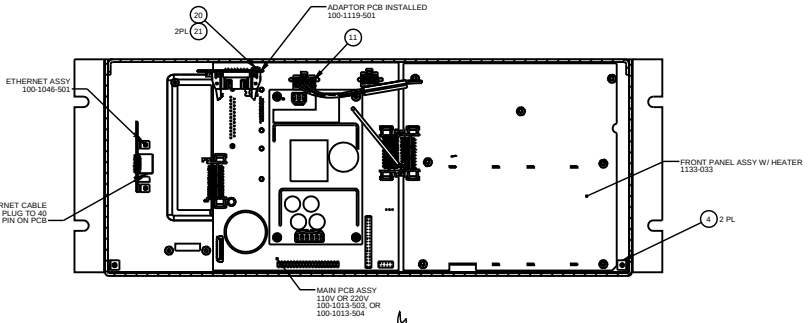
1. SEE MWI-09-195 FOR TYPE 1 RACKMOUNT CONTROLLER [100-0000-510].

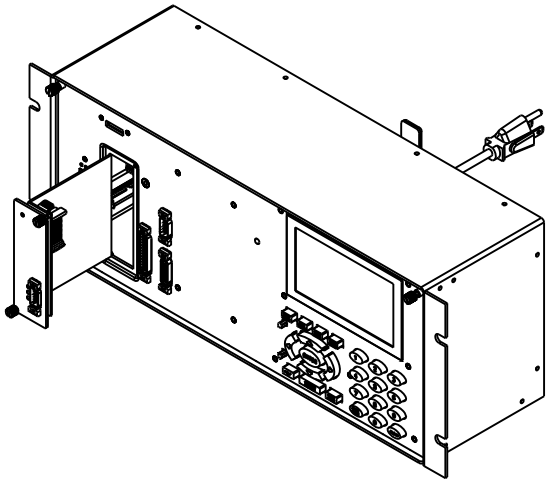
ECONOLITE CONTROL PRODUCTS, INC.
3360 E. La PALMA, ANAHEIM, CA. 92806

TITLE: **UNIT ASSY, ASC/3**

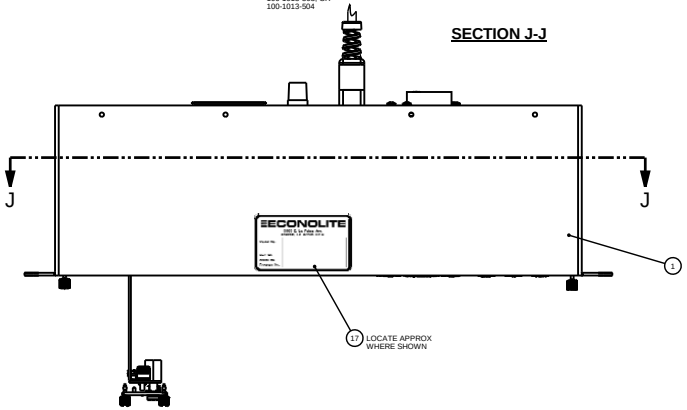
SIZE	CAGE CODE	DRAWING NO.	REV
D	0FEW7	100-0000-5XX	H

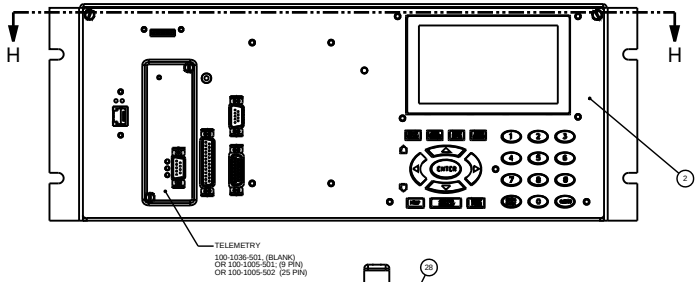
SCALE: 1:1 | SHEET SIZE: 100-0000-5XX.SLDDRW | Sheet 2 OF 3

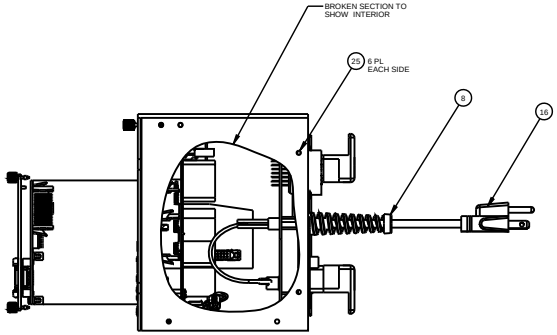


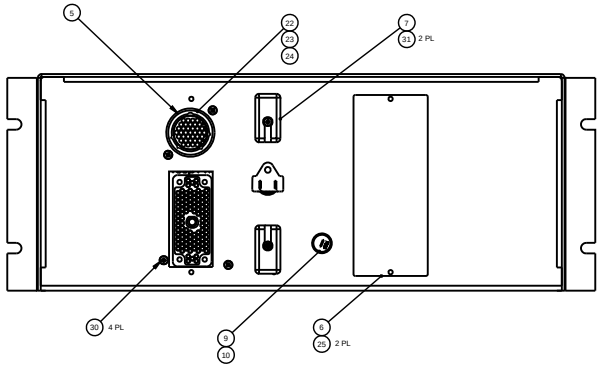


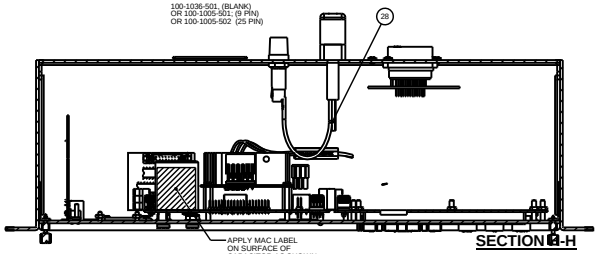
SECTION J-J











SECTION H-H

511 SHOWN

2. SEE MWI-09-196 FOR TYPE 2 RACKMOUNT CONTROLLER [100-0000-511].

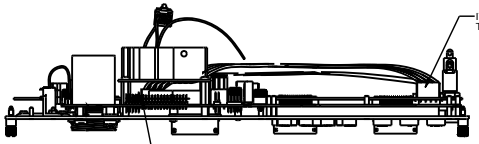
ECONOLITE CONTROL CONTINUITY, INC.
3360 E. La PALMA, ANAHEIM, CA. 92806

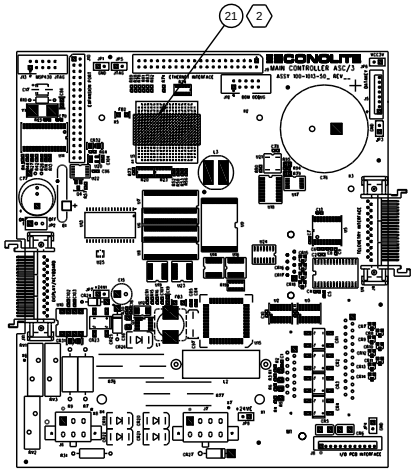
TITLE: **UNIT ASSY, ASC/3**

SIZE	CAGE CODE	DRAWING NO.	REV
D	0FEW7	100-0000-5XX	H

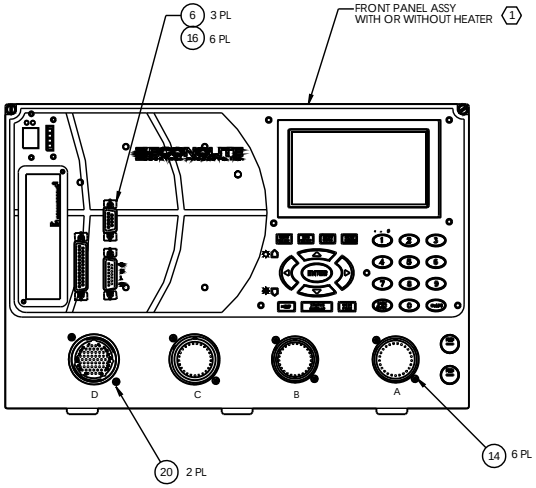
SCALE: 1:2 | SHEET SIZE: 100-0000-5XX.SLDDRW | Sheet 3 OF 3

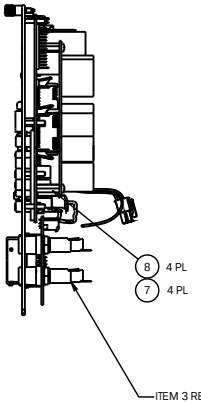
REVISIONS				
REV.	BY	E.C.O. NUMBER	DATE	APPROVED
NC	MC	INITIAL RELEASE, SEE ECO 21271	9-8-04	J.G.
A	MC	SEE ECO 21380	12-08-04	J.G.
B	MC	SEE ECO 21401	1-5-05	J.G.
C	MC	SEE ECO 21445	2-23-05	J.G.
D	MC	SEE ECO 21718	9-12-05	J.G.
E	MC	SEE ECO 21836	1-6-06	J.R.
F	MC	SEE ECO 21929	3-28-06	J.R.
G	MC	SEE ECO 21994	5-2-06	J.R.
H	MC	SEE ECO 22398	5-31-07	J.R.
J	MC	SEE ECO 22591	11-20-07	J.R.
K	MC	SEE ECO 22601	11-20-07	J.R.

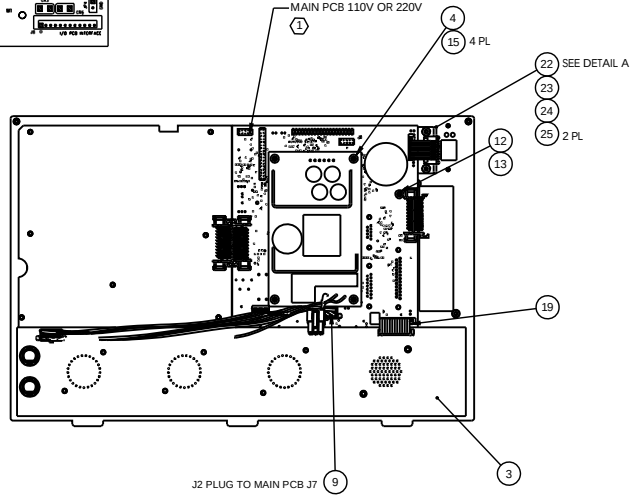




DETAIL VIEW- MAIN PCB







-502

2 INSTALL SOFTWARE LABEL, ITEM 21, REF WORK INSTRUCTION MWI-09-54 FOR -502 & MWI-09-53 FOR -501.

1 INSTALL NOTED PARTS PER CONFIGURATION BILL OF MATERIAL.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	DESCRIPTION
-502	ASSY, FRONT PNL, TS2 TYPE 2, ASC/3
-501	ASSY, FRONT PNL, TS2 TYPE 1, ASC/3

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONS ± DECIMAL ± ANGULAR ±
BREAK SHARP EDGES
PART MUST BE FREE OF ANY FOREIGN CONTAMINANTS.

DRAWN	M. CHU	5-19-04
ENGR	M. CHU	5-19-04
CHK'D	G. ROS	5-19-04
APVD'D	J. GROSS	5-19-04
MFG	E. RAAMOT	9-1-04
MATERIAL		
FINISH		

DO NOT SCALE DRAWING

MODEL FILE: 100-1030-502.SLDPRT

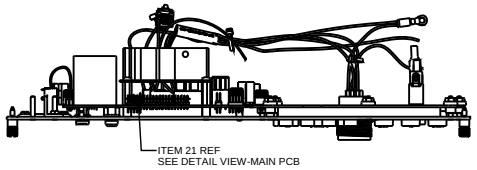
ECONOLITE CONTROL PRODUCTS, INC.
ANGEL 1st PALMA, ANAHEIM, CA. 92806

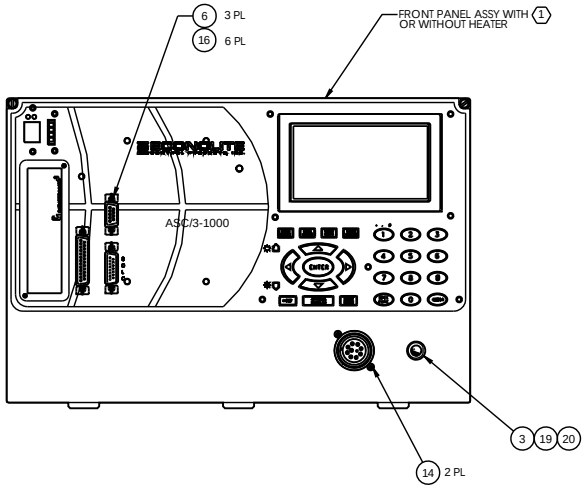
TITLE: ASSY, FRONT PANEL TS2, ASC/3

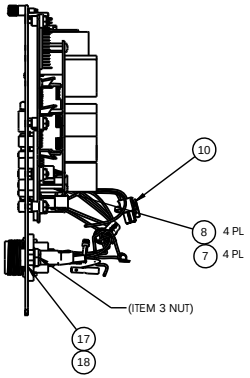
SIZE	CAGE CODE	DRAWING NO.	REV.
D	0FEW7	100-1030-5XX	K

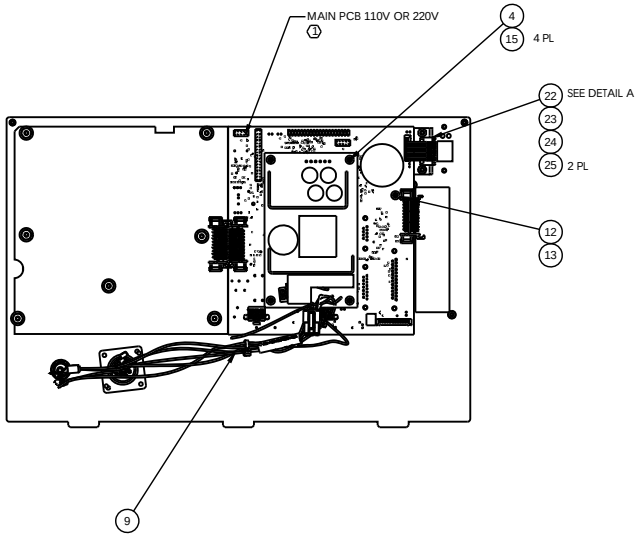
SCALE: 1:1 | CAD FILE: 100-0300-500.SLDDRW | Sheet 1 OF 2

K
100-1030-5XX
D









.15

CABLE BENDING DETAIL

BEND THE .25 LONG LEADS OF RIBBON CABLE (ITEM 23) AS SHOWN.
AND SOLDER TO RECEPTACLE (ITEM 22).

-501

DETAIL A

ECONOLITE CONTROL PRODUCTS, INC.
1360 E. La PALMA, ANAHEIM, CA. 92806

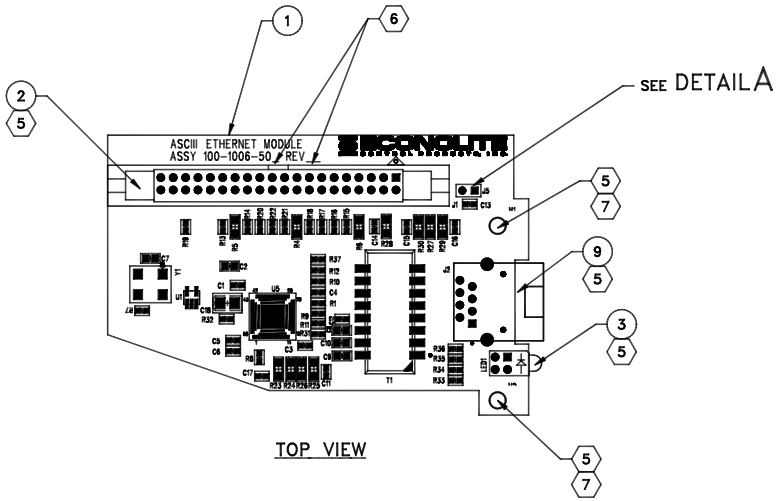
TITLE: ASSY, FRONT PANEL TS2, ASC/3

SIZE	CAGE CODE	DRAWING NO.	REV
D	0FEW7	100-1030-5XX	K

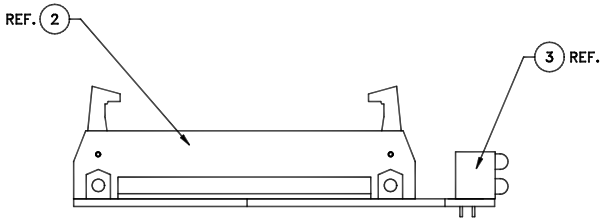
SCALE: 1:2 | SHEET SIZE: 100-1030-5XX.SLDDRW | Sheet 2 OF 2

100-1030-5XX
K
D

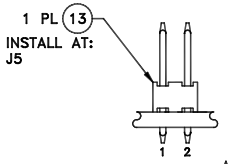
REVISIONS				
REV	ZONE	DESCRIPTION	APPD/DATE	E.O. NO.
NC		INITIAL RELEASE – REV. NC IS THE SAME AS REV. 1	[illegible]	21200
A		SEE ECO	[illegible]	21270
B		SEE ECO	[illegible]	21427
C		SEE ECO	[illegible]	21510
D		SEE ECO	[illegible]	21867



TOP VIEW



FRONT VIEW



DETAIL A
SCALE 4:1

(7) ALL MOUNTING HOLES TO BE FREE OF SOLDER.

(6) INSTALL LABEL CONTAINING ASSEMBLY NUMBER & REVISION LETTER. LABEL SHALL USE .12" HIGH CHARACTERS.

(5) AREAS TO BE FREE OF ALL CONFORMAL COATING, SHALL BE INSPECTED USING A BLACK LIGHT INSPECTION STATION OR EQUIVALENT. THE AREAS ARE AS FOLLOWS: ALL TEST POINTS, ALL CONNECTORS, ALL SOCKETS, ALL SWITCHES AND MOUNTING HOLE PADS.

4. AFTER ASSEMBLY AND SOLDERING OF COMPONENTS, MOISTURE AND FUNGUS PROOF BOTH SIDES OF P.C. BOARD WITH HUMISEAL 1B73 OR EQUIVALENT TO MIN. THICKNESS OF .002

3. ASSEMBLE AND SOLDER COMPONENTS. DO NOT CLINCH PARTS LEADS (REF 33729).

2. REFERENCE DESIGNATIONS SHOWN ARE FOR LOCATING PURPOSES ONLY.

1. REF. SCHEMATIC DRAWING NO. 100-1006-601

NOTES: UNLESS OTHERWISE SPECIFIED

501 SHOWN

501	ASSY., PCB, ASC/3 ETHERNET BD.
DASH NO.	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS .XX ± .03 .XXX ± .015
ANGLES ± 30'
DO NOT SCALE DRAWING
DRILLED HOLE
.015 – .125 ± .003
.126 – .390 ± .005
.391 – .690 ± .007
.691 – .780 ± .009
.781 – 1.000 ± .010
1.001 – 2.000 ± .012

MATERIAL:
FINISH:

DRAWN	GREG RIOS	7-01-04
CHECKED	H. PATEL	7-16-04
ENGINEER	J. GROSS	7-16-04
APPROVED	E. RAAMOT	7-19-04

ECONOLITE CONTROL PRODUCTS, INC. 3360 E. LA PALMA ANAHEIM, CALIFORNIA 92806

TITLE: ASSY., PCB, ASC/3 ETHERNET MODULE BOARD

SCALE	F.S.F.	SHEET	SIZE	DRAWING NO.	REV
2:1		1 OF 1	D	100-1006-5XX	D

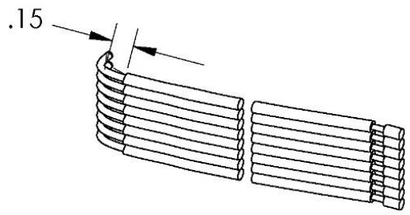
F1008

REV D | DRAWING NO. 100-1006-5XX | SIZE D | SHEET 1 OF 1

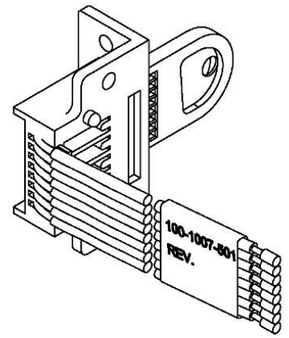
REVISIONS				
REV.	BY	E.C.O. NUMBER	DATE	APPRD
NC	MC	21287	9-29-04	J.G.

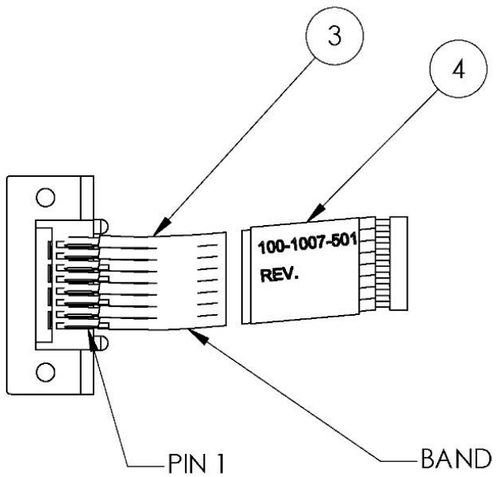
NOTES: (UNLESS OTHERWISE SPECIFIED)

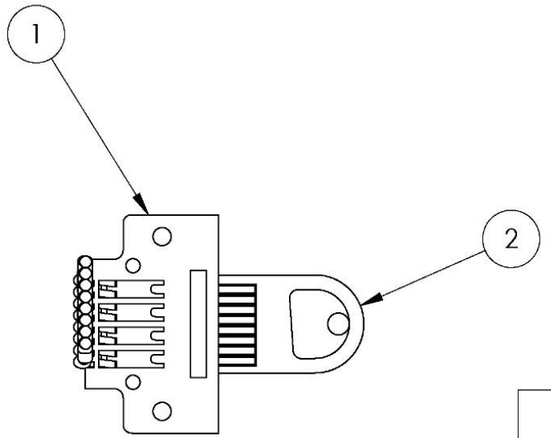
1. BEND THE .25 LONG LEADS OF RIBBON CABLE (ITEM 3) AS SHOWN, & SOLDER TO RECEPTACLE (ITEM 1).
2. IDENTIFY PER ECONOLITE MFG PROCEDURE 33552.



CABLE BENDING DETAIL







501	ASSY, DATA MODULE KIT, ASC/3
DASH NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DEBURR AND BREAK ALL SHARP EDGES
PART MUST BE FREE OF ANY FOREIGN CONTAMINANTS.

TOLERANCE
DECIMAL: XX ± .03, XXX ± .015
ANGULAR: ± 0°30'

DRAWN	M. CHU	8-26-04
DESIGN	M. CHU	8-26-04
CHECK	G. RIOS	9-17-04
ENGINEER	J. GROSS	9-17-04
APPRD	M. De LANGE	9-17-04
MATERIAL		
FINISH		

MODEL FILE: datakey.SLDPRT

DO NOT SCALE DRAWING

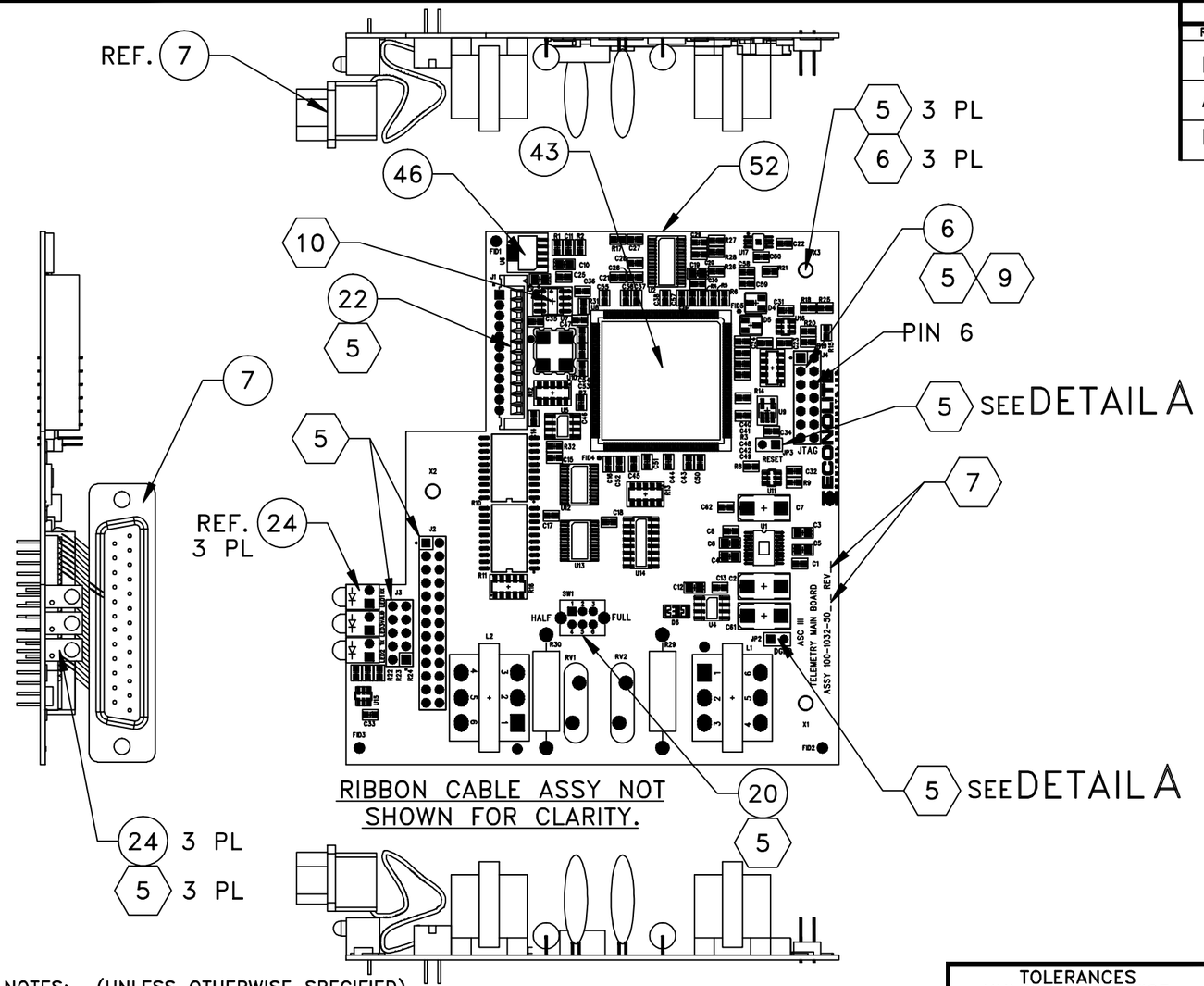
ECONOLITE CONTROL PRODUCTS, INC.
3360 E. La PALMA, ANAHEIM, CA. 92806

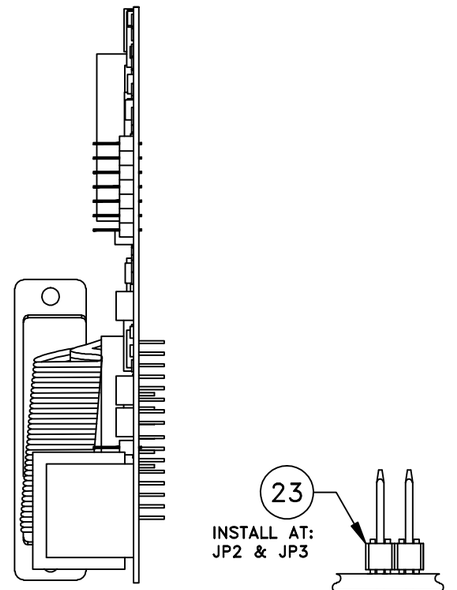
TITLE
ASSY, DATA MODULE, KIT ASC/3

SIZE	CAGE CODE	DRAWING NO.	REV.
B	0FEW7	100-1007-5XX	NC

SCALE: 2:1 | CAD FILE: 100-1007-5XX.SLDDRW | Sheet 1 OF 1

REVISIONS				
REV.	ZONE	DESCRIPTION	APPD/DATE	E.O. NO.
NC		INITIAL RELEASE – REV. NC IS THE SAME AS REV. 1	J. GROSS 8-17-05	21330
A		SEE ECO	J. ROSE 12-19-05	21805
B		SEE ECO	J. ROSE 12-20-05	21817





501 SHOWN

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. REF. SCHEMATIC DRAWING NO. 100-1032-601.
2. REFERENCE DESIGNATIONS SHOWN ARE FOR LOCATING PURPOSES ONLY.
3. ASSEMBLE AND SOLDER COMPONENTS. DO NOT CLINCH PARTS LEADS (REF. 33729).
4. AFTER ASSEMBLY AND SOLDERING OF COMPONENTS, MOISTURE AND FUNGUS PROOF BOTH SIDES OF P.C. BOARD WITH HUMISEAL 1B73 OR EQUIVALENT TO MIN. THICKNESS OF .002
5. AREAS TO BE FREE OF ALL CONFORMAL COATING, SHALL BE INSPECTED USING A BLACK LIGHT INSPECTION STATION OR EQUIVALENT. THE AREAS ARE AS FOLLOWS: ALL TEST POINTS, ALL CONNECTORS, ALL SOCKETS, ALL SWITCHES, ALL MOUNTING HOLE PADS, ALL LEDS, AND ALL JUMPERS.
6. ALL MOUNTING HOLES TO BE FREE OF SOLDER.
7. MARK ASSY. NUMBER & REVISION LETTER OF ASSEMBLY IN .12 HIGH CHARACTERS.
8. COLORED BAND DENOTES CATHODE END OF DIODE.
9. CLIP PIN 6 ON J4.
10. BEFORE ASSEMBLY IC U7 SHALL BE PROGRAMMED WITH SOFTWARE 100-1073-001.

DASH #	DESCRIPTION
502	ASSY, PCB, TELEMETRY, MAIN, 9 PIN, ASC/3
501	ASSY, PCB, TELEMETRY, MAIN, 25 PIN, ASC/3

TOLERANCES UNLESS OTHERWISE SPECIFIED

DECIMALS		ANGLES
± .03 .XX	± .015 .XXX	± 30'

DO NOT SCALE DRAWING

DRILLED HOLE

.013 – .125	+ .004 – .001
.126 – .250	+ .005 – .001
.251 – .500	+ .006 – .001
.501 – .750	+ .008 – .001
.751 – 1.000	+ .010 – .001
1.001 – 2.000	+ .012 – .001

MATERIAL:

FINISH:

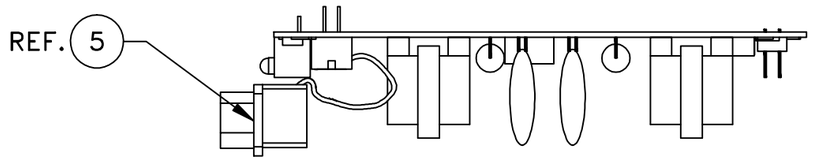
		DATE
DRAWN	GREG RIOS	5-9-05
CHECKED	H. PATEL	5-11-05
ENGINEER	J. GROSS	5-11-05
APPROVED	G. DUNCAN	5-11-05

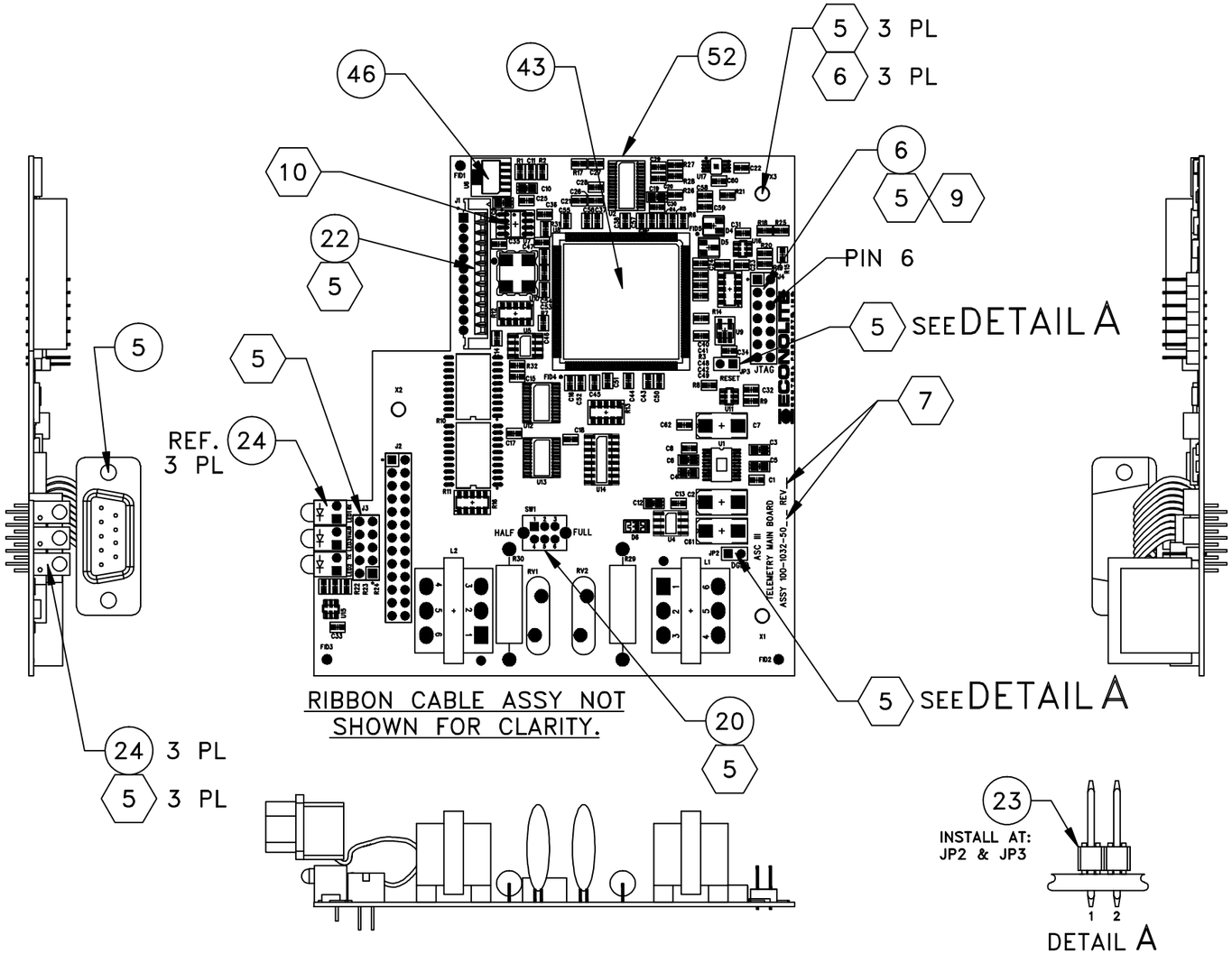
ECONOLITE CONTROL PRODUCTS. INC.
3360 E. LA PALMA
ANAHEIM, CALIFORNIA 92806

TITLE

ASSY, PCB, TELEMETRY, MAIN, ASC/3

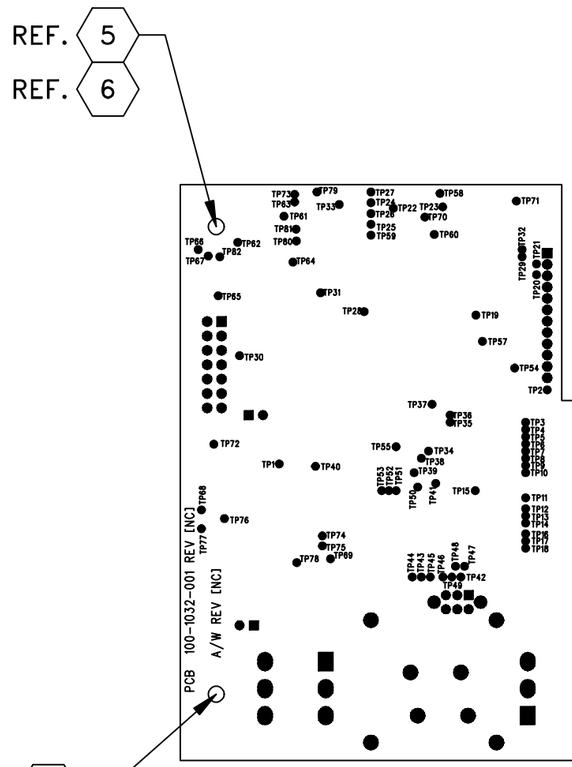
SCALE	F.C.F.	SHEET	SIZE	DRAWING NO.	REV
1:1		1 OF 2	B	100-1032-5XX	B





RIBBON CABLE ASSY NOT SHOWN FOR CLARITY.

DETAIL A
SCALE 2:1



501/502 SHOWN
REAR VIEW

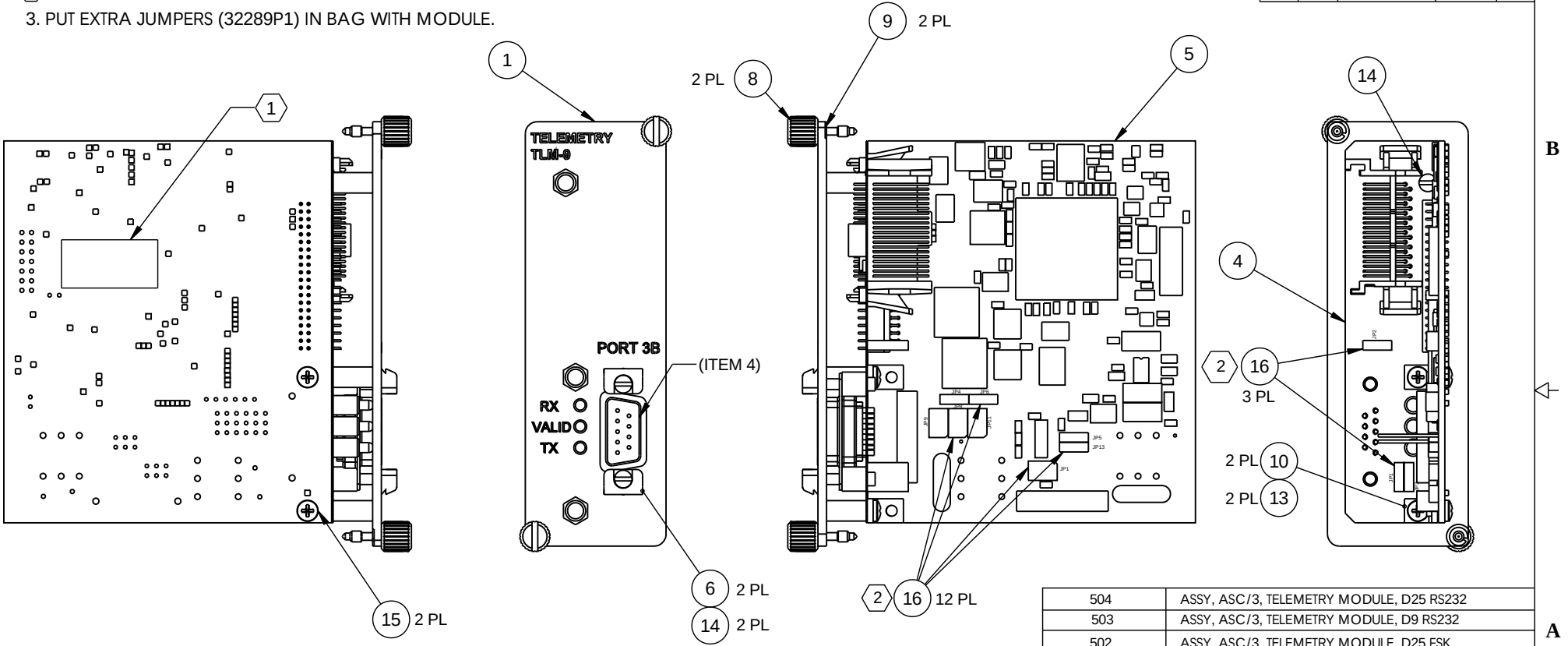
502 SHOWN

SCALE	F.C.F.	SHEET	SIZE	DRAWING NO.	REV
1:1		2 of 2	B	100-1032-5XX	B

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. LABEL MARKED WITH PART# AND REV. BRADY# LAT-7-7-99.
2. FOR JUMPER INSTALLATION SEE SHEET 3 CONFIGURATIONS.
3. PUT EXTRA JUMPERS (32289P1) IN BAG WITH MODULE.

REVISIONS				
REV.	BY	E.C.O. NUMBER	DATE	APPRD
NC	MC	22368	4/26/07	J.R.
A	GR	22806	5-16-08	J.R.
B	GR	22858	5-27-08	J.R.



-501/-503

DASH No.	DESCRIPTION
504	ASSY, ASC/3, TELEMETRY MODULE, D25 RS232
503	ASSY, ASC/3, TELEMETRY MODULE, D9 RS232
502	ASSY, ASC/3, TELEMETRY MODULE, D25 FSK
501	ASSY, ASC/3, TELEMETRY MODULE, D9 FSK

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DEBURR AND BREAK ALL SHARP EDGES
PART MUST BE FREE OF ANY FOREIGN CONTAMINANTS
TOLERANCE
DECIMAL: XX ± .03, XXX ± .015
ANGULAR: ± 0°30'

DRAWN	M. CHU	2-14-07
DESIGN	M. CHU	2-14-07
CHECK	R. McLENDON	3-14-07
ENGINEER	J. ROSE	3-14-07
APPRD	E. RAAMOT	3-14-07
MATERIAL		
FINISH		

MODEL FILE: 100-1084-501.SLDPRT

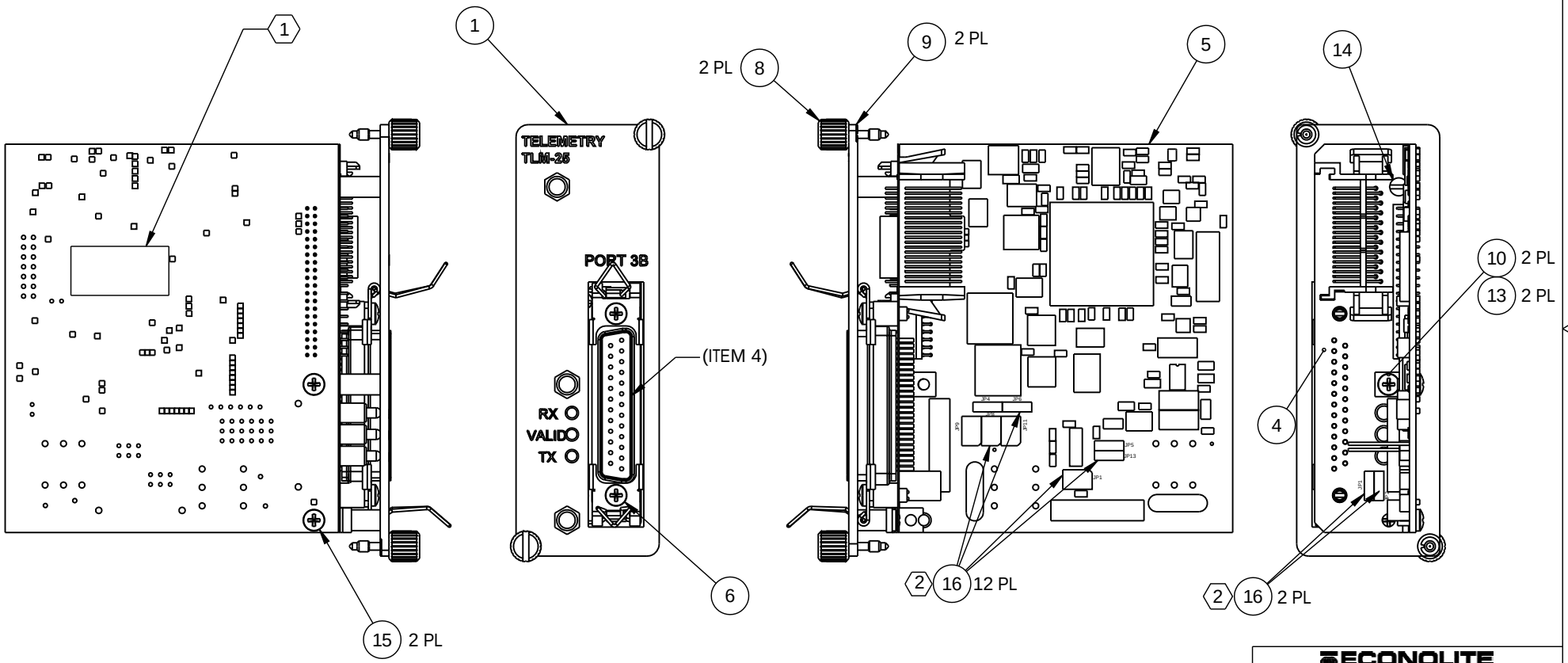
DO NOT SCALE DRAWING

ECONOLITE CONTROL PRODUCTS, INC.
3360 E. La PALMA, ANAHEIM, CA. 92806

TITLE: ASSY, ASC/3, TELEMETRY MODULE

SIZE	CAGE CODE	DRAWING NO.	REV.
B	0FEW7	100-1084-5XX	B

SCALE: 1:2 | CAD FILE: 100-1084-5XX.SLDDRW | Sheet 1 OF 3



-502/-504

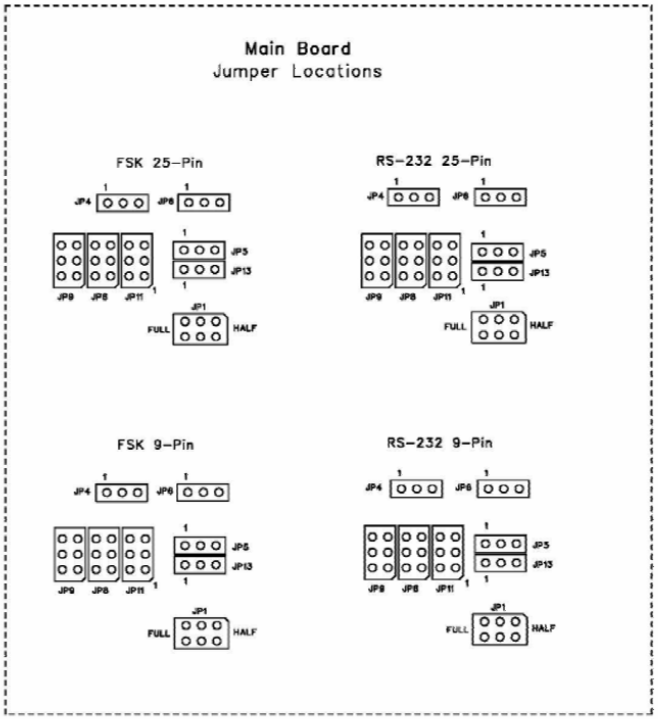
ECONOLITE CONTROL PRODUCTS, INC.
3360 E. La PALMA ANAHEIM, CA 92806

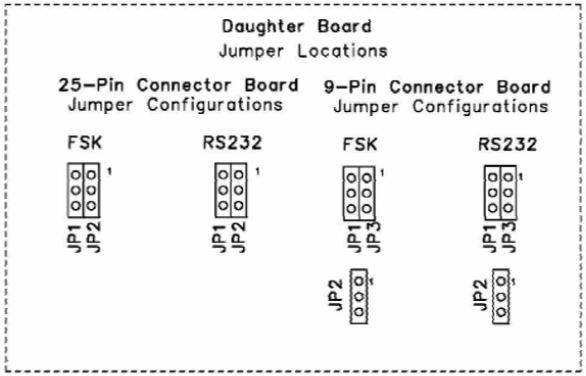
ASSY, ASC/3, TELEMETRY MODULE

DO NOT SCALE DRAWING

SIZE	CAGE CODE	DRAWING NO.	REV.
B	0FEW7	100-1084-5XX	B

SCALE: 1:2 | CAD FILE: 100-1084-5XX.SLDDRW | SHEET 2 OF 3





Refer to schematic 100-1093-601 Latest Revision for jumper setting

ECONOLITE CONTROL PRODUCTS, INC.
3360 E. La PALMA ANAHEIM, CA 92806

ASSY, ASC/3,
TELEMETRY MODULE

DO NOT SCALE DRAWING

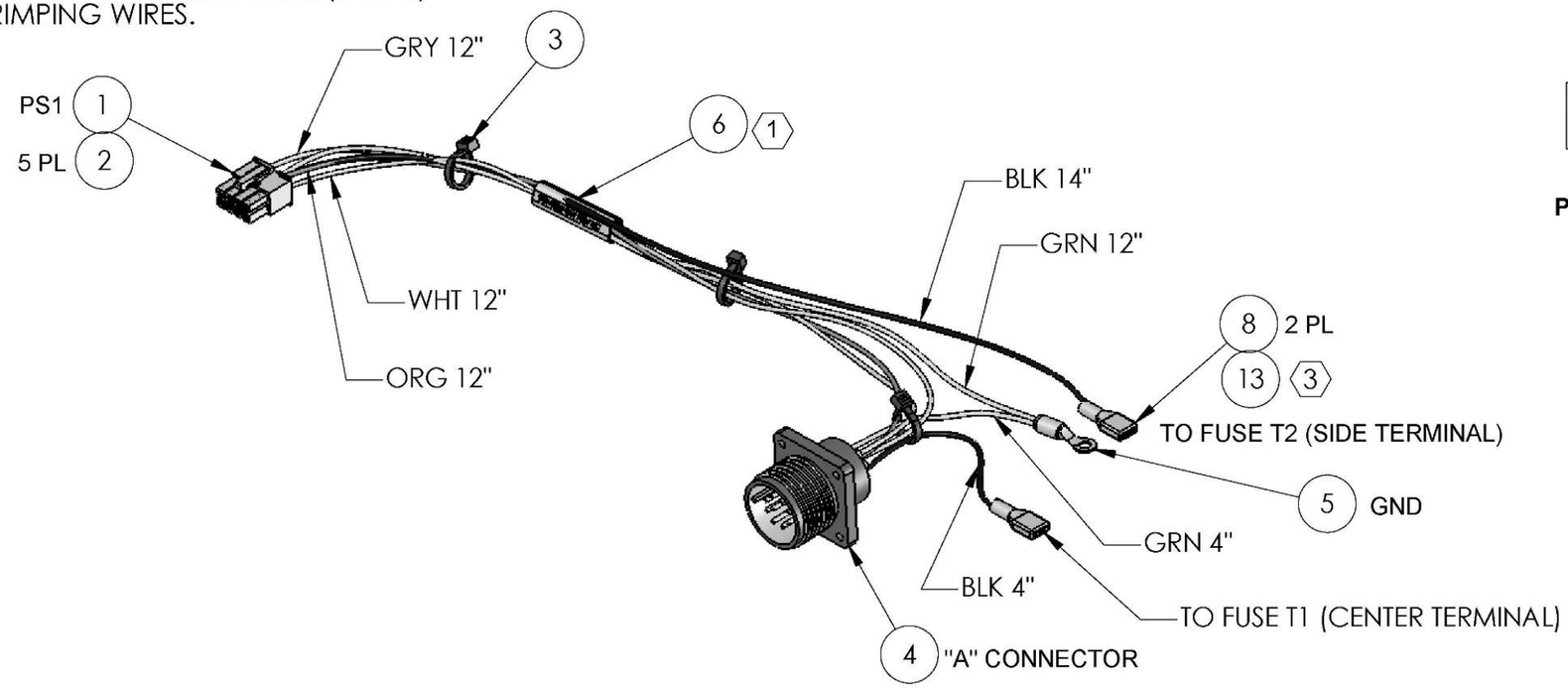
SIZE	CAGE CODE	DRAWING NO.	REV.
B	0FEW7	100-1084-5XX	B

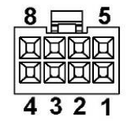
SCALE: 1:2 | CAD FILE: 100-1084-5XX.SLDDRW | SHEET 3 OF 3

NOTES: (UNLESS OTHERWISE SPECIFIED)

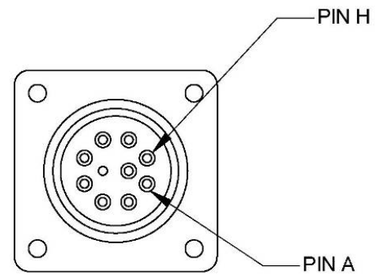
1. IDENTIFY PER ECONOLITE MFG PROCEDURE 33552.
2. FOR REV SEE BOM.
3. APPLY SHRINK TUBING (ITEM 13) TO COVER ALL OF THE QUICK DISCONNECTS (ITEM 8) AFTER CRIMPING WIRES.

REVISIONS				
REV.	BY	E.C.O. NUMBER	DATE	APPRD
NC	MC	SEE ECO # 20998	4-2-04	JG
A	MC	SEE ECO # 21059	5-4-04	JG





P1 BACK VIEW



"A" CONNECTOR BACK VIEW

WIRE LIST (ALL WIRE ARE 18 AWG)					
PS1 PIN#	WIRE COLOR	WIRE LENGTH	FUSE	GND RING	"A" CONN JX1 PIN# / FUNCTION
1	BLK	14"	T-2		
2	WHT	12"			A / NEUTRAL
3	GRN	12"		GND	
5	GRY	12"			G / FGND
7	ORG	12"			F /FAULTMON
	BLK	4"	T-1		C / LINE
	GRN	4"		GND	H /EARTH

501	ASSY, CABLE, POWER, TS2-1
DASH #	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DEBURR AND BREAK ALL SHARP EDGES
PART MUST BE FREE OF ANY FOREIGN CONTAMINANTS

TOLERANCE
DECIMAL: XX ± .03, XXX ± .015
ANGULAR: ± 0°30'

DRAWN	M. CHU	12-29-03
DESIGN	M. CHU	12-29-03
CHECK	R. McLENDON	1-8-04
ENGINEER	J. GROSS	1-8-04
APPRD	J. GROSS	4-2-04
MATERIAL		
FINISH		

ECONOLITE CONTROL PRODUCTS, INC.
3360 E. La PALMA, ANAHEIM, CA. 92806

TITLE: ASSY, CABLE, POWER, TS2-1

SIZE	CAGE CODE	DRAWING NO.	REV.
B	0FEW7	100-1020-5XX	A

SCALE: 1:2 | CAD FILE: 100-1020-5XX.SLDDRW | Sheet 1 OF 1

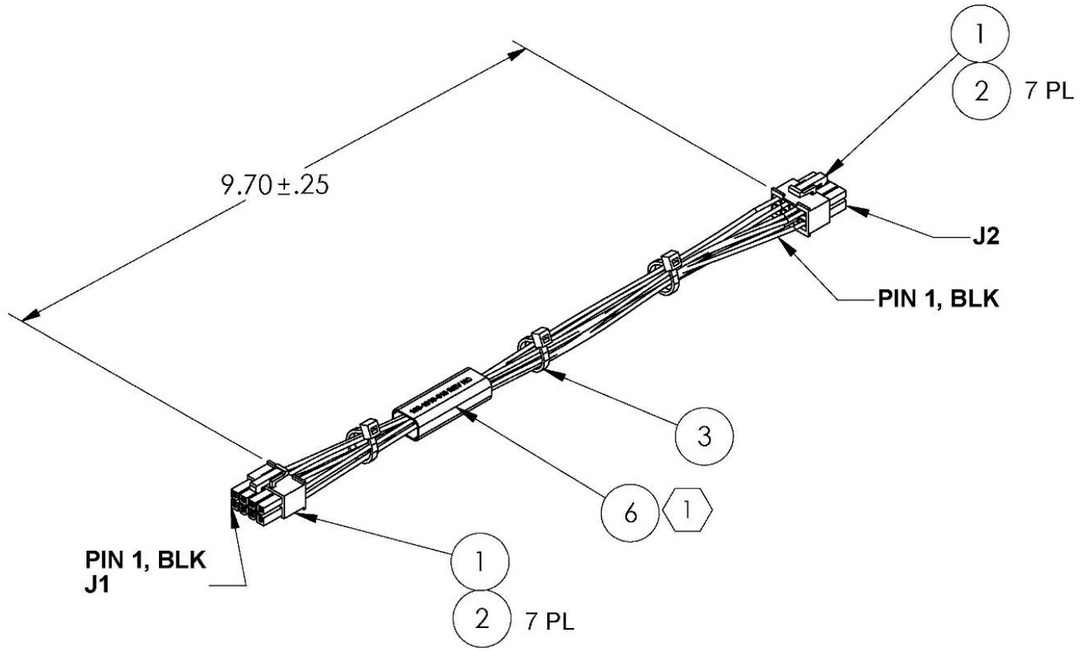
MODEL FILE: cableassy_pwr ts2.SLDPRT

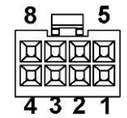
DO NOT SCALE DRAWING

NOTES: (UNLESS OTHERWISE SPECIFIED)

(1) IDENTIFY PER ECONOLITE MFG PROCEDURE 33552.

REVISIONS				
REV.	BY	E.C.O. NUMBER	DATE	APPRD
NC	MC	SEE ECO# 20998	4-2-04	JG
A	MC	SEE ECO# 21237	8-9-04	JG





J1/J2 BACK VIEW

WIRE LIST				
(JI) PIN#	LENGTH	AWG	COLOR	(J2) PIN#
1	10.5"	#18	BLK	1
2	10.5"	#18	WHT	2
3	10.5"	#18	GRN	3
4	NC			4
5	10.5"	#18	GRY	5
6	10.5"	#18	GRY	6
7	10.5"	#18	ORG	7
8	10.5"	#18	RED	8

501	NC	ASSY, CABLE, TS2-2
DASH #	REV	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DEBURR AND BREAK ALL SHARP EDGES
PART MUST BE FREE OF ANY FOREIGN CONTAMINANTS

TOLERANCE
DECIMAL: X ± .2, XX ± .03, XXX ± .015
ANGULAR: ± 0°30'

DRAWN	M. CHU	12-29-03
DESIGN	M. CHU	12-29-03
CHECK	R. McLENDON	1-6-04
ENGINEER	J. GROSS	1-6-04
APPRD		
MATERIAL		
FINISH		

ECONOLITE CONTROL PRODUCTS, INC.
3360 E. La PALMA, ANAHEIM, CA. 92806

TITLE: ASSY, CABLE, TS2-2

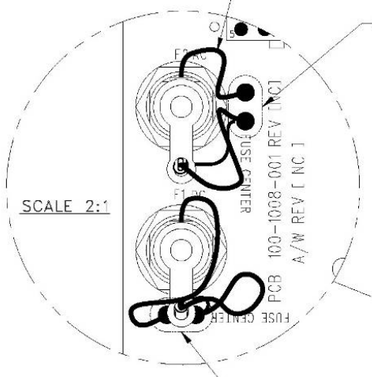
SIZE	CAGE CODE	DRAWING NO.	REV.
B	0FEW7	100-1019-5XX	A

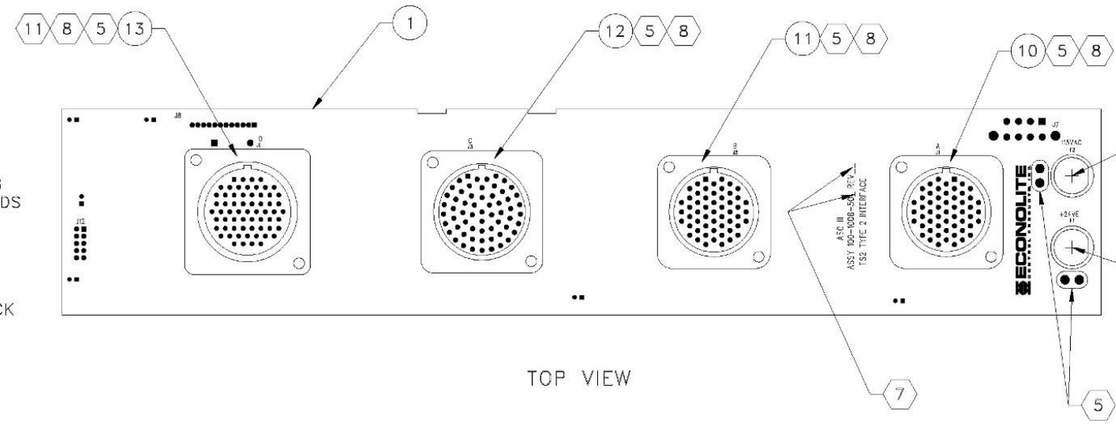
SCALE: 1:2 | CAD FILE: 100-1019-5XX.SLDDRW | Sheet 1 OF 1

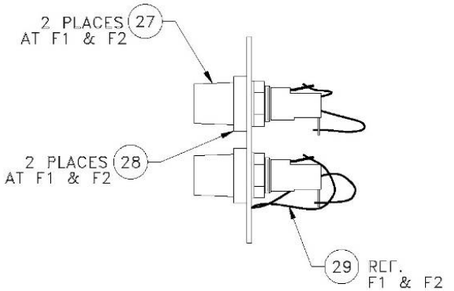
MODEL FILE: ASSY_CABLE8.SLDPRT

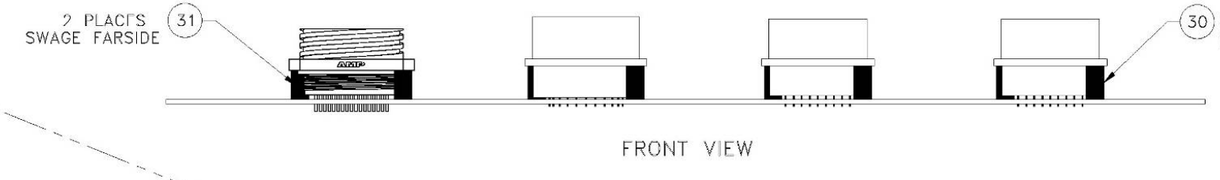
DO NOT SCALE DRAWING

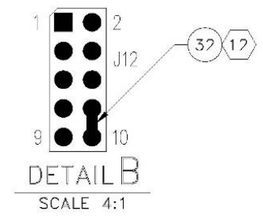
REVISIONS				
REV	ZONE	DESCRIPTION	APPD/DATE	E.C. NO.
NC		INITIAL RELEASE – REV. NC IS THE SAME AS REV. 2	J. GROSS 7-27-04	21200
A		SEE ECO	J. GROSS 7-3-05	21436
B		SEE ECO	J. GROSS 3-21-05	21486
C		SEE ECO	J. GROSS 4-20-05	21542











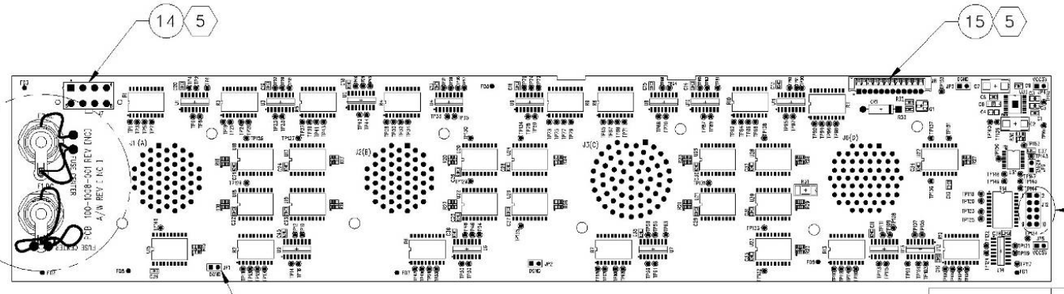
29 CUT INTO (4) 2" LONG WIRES, STRIP BOTH ENDS .125 AND TIN, THEN INSTALL AS SHOWN.

5 TOP & BACK OF PCB

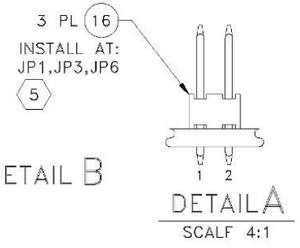
5 TOP & BACK OF PCB

12. ADD JUMPER ITEM 32 ON J12 BETWEEN PIN8 AND PIN10.
11. REMOVE PIN7 ON J6 PRIOR TO ASSEMBLY.
10. INSTALL ALL DIODES PER CATHODE SILKSCREEN ON CIRCUIT BOARD.
9. COLORED BAND DENOTES CATHODE END OF DIODE.
8. ALL MOUNTING HOLES TO BE FREE OF SOLDER.
7. INSTALL LABEL CONTAINING ASSEMBLY NUMBER & REVISION LETTER. LABEL SHALL USE .12" HIGH CHARACTERS.
6. INSTALL AFTER WAVE SOLDER AND CONFORMAL COATING.
5. AREAS TO BE FREE OF ALL CONFORMAL COATING, SHALL BE INSPECTED USING A BLACK LIGHT INSPECTION STATION OR EQUIVALENT. THE AREAS ARE AS FOLLOWS: ALL TEST POINTS, ALL CONNECTORS, ALL SOCKETS, ALL SWITCHES AND MOUNTING HOLE PADS.
4. AFTER ASSEMBLY AND SOLDERING OF COMPONENTS, MOISTURE AND FUNGUS PROOF BOTH SIDES OF P.C. BOARD WITH HUMISEAL 1B73 OR EQUIVALENT TO MIN. THICKNESS OF .002
3. ASSEMBLE AND SOLDER COMPONENTS. DO NOT CLINCH PARTS LEADS (REF 33729).
2. REFERENCE DESIGNATIONS SHOWN ARE FOR LOCATING PURPOSES ONLY.
1. REF. SCHEMATIC DRAWING NO. 100-1008-601

NOTES: UNLESS OTHERWISE SPECIFIED



501 SHOWN
BACK VIEW



501	ASSY., PCB, ASC/3 TS2 TYPE 2 CONNECTOR BD.
DASH NO.	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS ± .03 .XX ± .015 .XXX ANGLES ± 30'
DO NOT SCALE DRAWING
DRILLED HOLE
.013 – .125 +.004 −.001
.126 – .750 +.005 −.001
.751 – .500 +.006 −.001
.501 – .750 +.008 −.001
.751 – 1.000 +.010 −.001
1.001 – 2.000 +.012 −.001

MATERIAL:
FINISH:

DRAWN	DATE
GREG RICS	5-24-04
CHECKED	
M. CHU	5-26-04
ENGINEER	
J. GROSS	7-14-04
APPROVED	
T. RAAMOT	7-19-04

ECONOLITE CONTROL PRODUCTS, INC. 3350 E. LA PALMA ANAHEIM, CALIFORNIA 92806

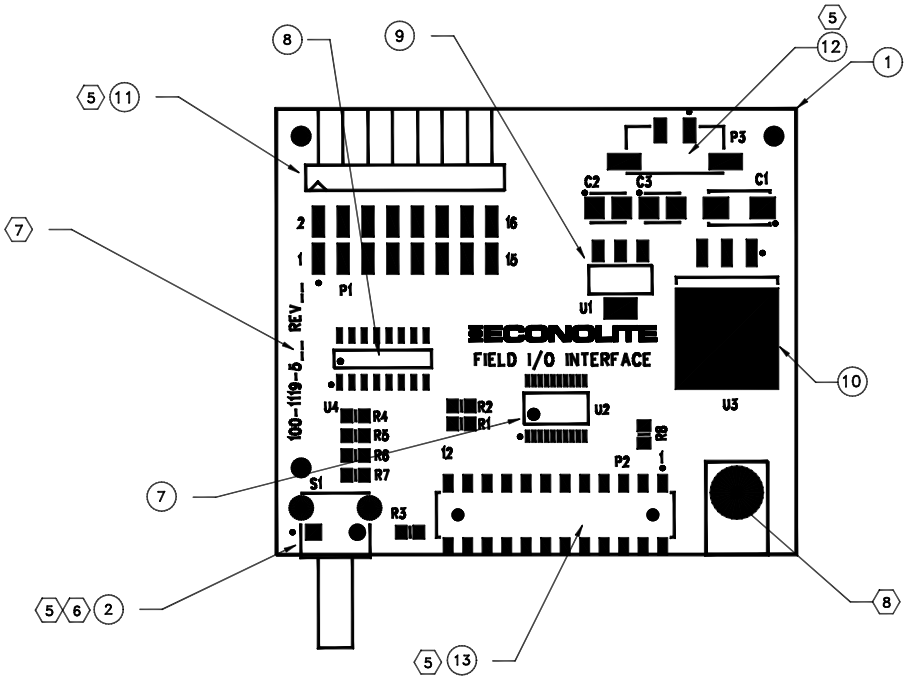
TITLE: ASSY., PCB, ASC/3 TS2 TYPE 2 CONNECTOR BOARD

SCALE 1:1 | SHEET 1 OF 1 | SIZE D | DRAWING NO. 100-1008-5XX | REV C

SIZE D | DRAWING NO. 100-1008-5XX | REV C | SHEET 1 OF 1

F1008

REVISIONS				
REV	ZONE	DESCRIPTION	APPR/DATE	E.O. NO.
NC		INITIAL RELEASE – REV. NC IS THE SAME AS REV. 1	J. ROSE 2-17-06	22829
A		SEE ECO	J. ROSE 10-31-06	23043



9. R4,6, AND S1 NOT INSTALLED.

(8) ALL MOUNTING HOLES TO BE FREE OF SOLDER.

(7) INSTALL LABEL CONTAINING ASSEMBLY NUMBER & REVISION LETTER. LABEL SHALL USE .12" HIGH CHARACTERS.

(6) INSTALL S1 AFTER SURFACE MOUNT SOLDER.

(5) AREAS TO BE FREE OF ALL CONFORMAL COATING, SHALL BE INSPECTED USING A BLACK LIGHT INSPECTION STATION OR EQUIVALENT. THE AREAS ARE AS FOLLOWS: ALL TEST POINTS, ALL CONNECTORS, ALL SOCKETS, ALL SWITCHES AND MOUNTING HOLE PADS.

4. AFTER ASSEMBLY AND SOLDERING OF COMPONENTS, MOISTURE AND FUNGUS PROOF BOTH SIDES OF P.C. BOARD WITH HUMISEAL 1B73 OR EQUIVALENT TO MIN. THICKNESS OF .002

3. ASSEMBLE AND SOLDER COMPONENTS. DO NOT CLINCH PARTS LEADS (REF 33729).

2. REFERENCE DESIGNATIONS SHOWN ARE FOR LOCATING PURPOSES ONLY.

1. REF. SCHEMATIC DRAWING NO. 100-1119-601

NOTES: UNLESS OTHERWISE SPECIFIED

501 SHOWN

501	ASSY., PCB, FIO INTERFACE, ASC/3
DASH	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMALS .XX ± .03, .XXX ± .015; ANGLES ± 30'

DO NOT SCALE DRAWING

DRILLED HOLE

.015 – .125	± .003
.126 – .390	± .004
.391 – .690	± .005
.691 – .790	± .006
.791 – 1.000	± .007
1.001 – 2.000	± .012

MATERIAL:

FINISH

DRAWN	M. CHU	4-17-06
CHECKED	S. LUU	4-17-06
ENGINEER	J. SHIELD	4-17-06
APPROVED	G. DUNCAN	4-17-06

ECONOLITE 3360 E. LA PALMA ANAHEIM, CALIFORNIA 92806

TITLE: ASSY., PCB, FIO INTERFACE, ASC/3

SCALE 4:1 | F.S.P. | SHEET 1 OF 1 | SIZE D | DRAWING NO. 100-1119-5XX | REV A

F1008

8. APPENDIX C: INTERFACE CONNECTOR PIN LISTS

CONNECTOR A 55 Pin (Plug) Type #22-55P			CONNECTOR B 55 Pin (Socket) Type #22-55S			CONNECTOR C 61 Pin (Socket) Type #24-61S		
PIN	FUNCTION	I/O	PIN	FUNCTION	I/O	PIN	FUNCTION	I/O
A	Fault Monitor	[O]	A	φ1 Phase Next	[O]	A	Status Bit A (Ring 2)	[O]
B	+24 VDC External	[O]	B	Preempt 2 Detector	[I]	B	Status Bit B (Ring 2)	[O]
C	Voltage Monitor	[O]	C	φ2 Phase Next	[O]	C	φ8 Don't Walk	[O]
D	φ1 Red	[O]	D	φ3 Green	[O]	D	φ8 Red	[O]
E	φ1 Don't Walk	[O]	E	φ3 Yellow	[O]	E	φ7 Yellow	[O]
F	φ2 Red	[O]	F	φ3 Red	[O]	F	φ7 Red	[O]
G	φ2 Don't Walk	[O]	G	φ4 Red	[O]	G	φ6 Red	[O]
H	φ2 Ped Clear	[O]	H	φ4 Ped Clear	[O]	H	φ5 Red	[O]
J	φ2 Walk	[O]	J	φ4 Don't Walk	[O]	J	φ5 Yellow	[O]
K	Vehicle Detector 2	[I]	K	φ4 Check	[O]	K	φ5 Ped Clear	[O]
L	Ped Detector 2	[I]	L	Vehicle Detector 4	[I]	L	φ5 Don't Walk	[O]
M	φ2 Hold	[I]	M	Ped Detector 4	[I]	M	φ5 Phase Next	[O]
N	Stop Time (Ring 1)	[I]	N	Vehicle Detector 3	[I]	N	φ5 Phase On	[O]
P	Inhibit MaxTerm(Ring1)	[I]	P	Ped Detector 3	[I]	P	Vehicle Detector 5	[I]
R	External Start	[I]	R	φ3 Phase Omit	[I]	R	Ped Detector 5	[I]
S	Interval Advance	[I]	S	φ2 Phase Omit	[I]	S	Vehicle Detector 6	[I]
T	Indicator Lamp Control	[I]	T	φ5 Ped Omit	[I]	T	Ped Detector 6	[I]
U	AC-Common	[I]	U	φ1 Phase Omit	[I]	U	Ped Detector 7	[I]
V	Chassis Ground	[I]	V	Ped Recycle(Ring 2)	[I]	V	Vehicle Detector 7	[I]
W	Logic Ground	[O]	W	Preempt 4 Detector	[I]	W	Ped Detector 8	[I]
X	Flashing Logic Out	[O]	X	Preempt 5 Detector	[I]	X	φ8 Hold Off	[I]
Y	Status Bit C (Ring1)	[O]	Y	φ3 Walk	[O]	Y	Force-Off (Ring 2)	[I]
Z	φ1 Yellow	[O]	Z	φ3 Ped Clear	[O]	Z	Stop Time (Ring 2)	[I]
a	φ1 Ped Clear	[O]	a	φ3 Don't Walk	[O]	a	Inhibit Max Term (Ring 2)	[I]
b	φ2 Yellow	[O]	b	φ4 Green	[O]	b	Test C	[I]
c	φ2 Green	[O]	c	φ4 Yellow	[O]	c	Status Bit C (Ring 2)	[O]
d	φ2 Check	[O]	d	φ4 Walk	[O]	d	φ8 Walk	[O]
e	φ2 Phase On	[O]	e	φ4 Phase On	[O]	e	φ8 Yellow	[O]
f	Vehicle Detector 1	[I]	f	φ4 Phase Next	[O]	f	φ7 Green	[O]
g	Ped Detector 1	[I]	g	φ4 Phase Omit	[I]	g	φ6 Green	[O]
h	φ1 Hold	[I]	h	φ4 Hold	[I]	h	φ6 Yellow	[O]
i	Force-Off (Ring 1)	[I]	i	φ3 Hold	[I]	i	φ5 Green	[O]
j	Ext Min Recall	[I]	j	φ3 Ped Omit	[I]	j	φ5 Walk	[O]
k	Manual Control Enable	[I]	k	φ6 Ped Omit	[I]	k	φ5 Check	[O]
m	Call To Non Actuate I	[I]	m	φ7 Ped Omit	[I]	m	φ5 Hold	[I]
n	Test A	[I]	n	φ8 Ped Omit	[I]	n	φ5 Phase Omit	[I]
p	AC+ (Control)	[I]	p	Overlap A Yellow	[O]	p	φ6 Hold	[I]
q	I/O Mode Bit A	[I]	q	Overlap A Red	[O]	q	φ6 Phase Omit	[I]
r	Status Bit B (Ring 1)	[O]	r	φ3 Check	[O]	r	φ7 Phase Omit	[I]
s	φ1 Green	[O]	s	φ3 Phase On	[O]	s	φ8 Phase Omit	[I]
t	φ1 Walk	[O]	t	φ3 Phase Next	[O]	t	Vehicle Detector 8	[I]
u	φ1 Check	[O]	u	Overlap D Red	[O]	u	Red Rest Mode (Ring 2)	[I]
v	φ2 Ped Omit	[I]	v	Preempt 6 Detector	[I]	v	Omit Red Clear (Ring 2)	[I]
w	Omit AllRed Clr(Ring1)	[I]	w	Overlap D Green	[O]	w	φ8 Ped Clear	[O]
x	Red Rest (Ring 1)	[I]	x	φ4 Ped Omit	[I]	x	φ8 Green	[O]
y	I/O Mode Bit B	[I]	y	Free (No Coord)	[I]	y	φ7 Don't Walk	[O]
z	Call To Non Act II	[I]	z	MaxII Select(Ring 2)	[I]	z	φ6 Don't Walk	[O]
AA	Test B	[I]	AA	Overlap A Green	[O]	AA	φ6 Ped Clear	[O]
BB	Walk Rest Modifier	[I]	BB	Overlap B Yellow	[O]	BB	φ6 Check	[O]
CC	Status Bit A (Ring 1)	[O]	CC	Overlap B Red	[O]	CC	φ6 Phase On	[O]
DD	φ1 Phase On	[O]	DD	Overlap C Red	[O]	DD	φ6 Phase Next	[O]
EE	φ1 Ped Omit	[I]	EE	Overlap D Yellow	[O]	EE	φ7 Hold	[I]
FF	Ped Recycle (Ring 1)	[I]	FF	Overlap C Green	[O]	FF	φ8 Check	[O]
GG	Max II Select(Ring 1)	[I]	GG	Overlap B Green	[O]	GG	φ8 Phase On	[O]
HH	I/O Mode Bit C	[I]	HH	Overlap C Yellow	[O]	HH	φ8 Phase Next	[O]
						JJ	φ7 Walk	[O]
						KK	φ7 Ped Clear	[O]
						LL	φ6 Walk	[O]
						MM	φ7 Check	[O]
						NN	φ7 Phase On	[O]
						PP	φ7 Phase Next	[O]

I/O MODE BITS (3 PER UNIT)

Mode	Bit States			State
#	**A**	**B**	**C**	**Names**
0	OFF	OFF	OFF	TS 1 Compatible
1	ON	OFF	OFF	Hardwire Interconnect
2	OFF	ON	OFF	System Interface
3	ON	ON	OFF	Reserved
4	OFF	OFF	ON	Reserved
5	ON	OFF	ON	Reserved
6	OFF	ON	ON	Manufacturer Specific
7	ON	ON	ON	Manufacturer Specific

Voltage Levels: OFF = +24; ON = 0V

MODE 0 INPUT/OUTPUT FUNCTIONS

Inputs:

Pin	Function
A-h	Phase 1 Hold
A-M	Phase 2 Hold
B-i	Phase 3 Hold
B-h	Phase 4 Hold
C-m	Phase 5 Hold
C-p	Phase 6 Hold
C-EE	Phase 7 Hold
C-X	Phase 8 Hold
B-U	Phase 1 Phase Omit
B-S	Phase 2 Phase Omit
B-R	Phase 3 Phase Omit
B-g	Phase 4 Phase Omit
C-n	Phase 5 Phase Omit
C-q	Phase 6 Phase Omit
C-r	Phase 7 Phase Omit
C-s	Phase 8 Phase Omit
A-EE	Phase 1 Ped Omit
A-v	Phase 2 Ped Omit
B-j	Phase 3 Ped Omit
B-x	Phase 4 Ped Omit
B-T	Phase 5 Ped Omit
B-k	Phase 6 Ped Omit
B-m	Phase 7 Ped Omit
B-n	Phase 8 Ped Omit

Outputs:

Pin	Function
A-DD	Phase 1 Phase On
A-e	Phase 2 Phase On
B-s	Phase 3 Phase On
B-e	Phase 4 Phase On
C-N	Phase 5 Phase On
C-CC	Phase 6 Phase On
C-NN	Phase 7 Phase On
C-GG	Phase 8 Phase On
B-A	Phase 1 Phase Next
B-C	Phase 2 Phase Next
B-t	Phase 3 Phase Next
B-f	Phase 4 Phase Next
C-M	Phase 5 Phase Next
C-DD	Phase 6 Phase Next
C-PP	Phase 7 Phase Next
C-HH	Phase 8 Phase Next
A-u	Phase 1 Check
A-d	Phase 2 Check
B-r	Phase 3 Check
B-K	Phase 4 Check
C-k	Phase 5 Check
C-BB	Phase 6 Check
C-MM	Phase 7 Check
C-FF	Phase 8 Check

MODE 1 INPUT/OUTPUT FUNCTIONS

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Vehicle Detector 9
B-h	Vehicle Detector 10
C-m	Vehicle Detector 13
C-p	Vehicle Detector 14
C-EE	Vehicle Detector 15
C-X	Vehicle Detector 16
B-U	Vehicle Detector 11
B-S	Vehicle Detector 12
B-R	Timing Plan C
B-g	Timing Plan D
C-n	Alternate Sequence A
C-q	Alternate Sequence B
C-r	Alternate Sequence C
C-s	Alternate Sequence D
A-EE	Dimming Enable
A-v	Automatic Flash
B-j	Timing Plan A
B-x	Timing Plan B
B-T	Offset 1
B-k	Offset 2
B-m	Offset 3
B-n	TBC On Line

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
C-N	Timing Plan A
C-CC	Timing Plan B
C-NN	Offset 1
C-GG	Offset 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
C-M	Offset 3
C-DD	Timing Plan C
C-PP	Timing Plan D
C-HH	Reserved
A-u	Free/Coord Status
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved
C-k	Reserved
C-BB	Reserved
C-MM	Reserved
C-FF	Reserved

MODE 2 INPUT/OUTPUT FUNCTIONS

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Vehicle Detector 9
B-h	Vehicle Detector 10
C-m	Vehicle Detector 13
C-p	Vehicle Detector 14
C-EE	Vehicle Detector 15
C-X	Vehicle Detector 16
B-U	Vehicle Detector 11
B-S	Vehicle Detector 12
B-R	Vehicle Detector 17
B-g	Vehicle Detector 18
C-n	Vehicle Detector 19
C-q	Vehicle Detector 20
C-r	Alarm 1
C-s	Alarm 2
A-EE	Dimming Enable
A-v	Local Flash Status
B-j	Address Bit 0
B-x	Address Bit 1
B-T	Address Bit 2
B-k	Address Bit 3
B-m	Address Bit 4
B-n	MMU Flash Status

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
C-N	Timing Plan A
C-CC	Timing Plan B
C-NN	Offset 1
C-GG	Offset 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
C-M	Offset 3
C-DD	Timing Plan C
C-PP	Timing Plan D
C-HH	Reserved
A-u	Free/Coord Status
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved
C-k	System Special Function 1
C-BB	System Special Function 2
C-MM	System Special Function 3
C-FF	System Special Function 4

Connector D

PIN	FUNCTION	I/O
25	SYSTEM COMMAND CYCLE BIT 1 INPUT	[I]
35	SYSTEM COMMAND CYCLE BIT 2 INPUT	[I]
6	SYSTEM COMMAND CYCLE BIT 3 INPUT	[I]
12	SYSTEM COMMAND OFFSET BIT 1 INPUT/	[I]
	EXTERNAL ADDRESS BIT 0	[I]
10	SYSTEM COMMAND OFFSET BIT 2 INPUT/	[I]
	EXTERNAL ADDRESS BIT 1	[I]
36	SYSTEM COMMAND OFFSET BIT 3 INPUT/	[I]
	EXTERNAL ADDRESS BIT 2	[I]
16	SYSTEM COMMAND SPLIT BIT 1 INPUT/	[I]
	EXTERNAL ADDRESS BIT 3	[I]
9	SYSTEM COMMAND SPLIT BIT 2 INPUT/	[I]
	EXTERNAL ADDRESS BIT 4	[I]
4	SYSTEM COMMAND COORD SYNC INPUT	[I]

NOTE: TX pins at the BIU are Rx pins at the controller. RX pins at the BIU are TX pins at the controller.

26	COORD FREE	[I]
60	AUTOMATIC FLASH	[I]
3	SPLIT DEMAND	[I]
38	DUAL COORD	[I]
14	TIME RESET	[I]
20	TEST INPUT C	[I]
37	TEST INPUT D	[I]
19	TEST INPUT E	[I]
57	PREEMPTOR CALL #1	[I]
49	PREEMPTOR CALL #2	[I]
50	PREEMPTOR CALL #3/BUS PREEMPTOR #1	[I]
55	PREEMPTOR CALL #4/BUS PREEMPTOR #2	[I]
56	PREEMPTOR CALL #5/BUS PREEMPTOR #3	[I]
61	PREEMPTOR CALL #6/BUS PREEMPTOR #4	[I]
58	CMU STOP TIME (CONFLICT FLASH)	[I]
17	EXPANDED DETECTOR #1	[I]
47	EXPANDED DETECTOR #2	[I]
31	EXPANDED DETECTOR #3	[I]
18	EXPANDED DETECTOR #4	[I]
30	EXPANDED DETECTOR #5	[I]
39	EXPANDED DETECTOR #6	[I]
40	EXPANDED DETECTOR #7	[I]
13	EXPANDED DETECTOR #8	[I]

NOTE: Priority preemptors 1 and 2 respond to any NEMA defined input applied to Preemptor Call input 1 and 2, respectively. Priority preemptors 3-6 respond to any NEMA defined input applied for at least 0.8 seconds to Preemptor Call inputs 3-6, respectively. Bus Preemptors 1-4 respond to a pulsing (1pps at 50% duty cycle) NEMA defined input applied to Preemptor Call input 3-6, respectively.

PIN	FUNCTION	I/O
43	SYSTEM COMMAND CYCLE BIT 1 OUTPUT	[O]
44	SYSTEM COMMAND CYCLE BIT 2 OUTPUT	[O]
29	SYSTEM COMMAND CYCLE BIT 3 OUTPUT	[O]
33	SYSTEM COMMAND OFFSET BIT 1 OUTPUT	[O]
42	SYSTEM COMMAND OFFSET BIT 2 OUTPUT	[O]
2	SYSTEM COMMAND OFFSET BIT 3 OUTPUT	[O]
21	SYSTEM COMMAND SPLIT BIT 1 OUTPUT	[O]
46	SYSTEM COMMAND SPLIT BIT 2 OUTPUT	[O]
53	SYSTEM COMMAND SYNC OUT	[O]
23	PREEMPTOR #1 ACTIVE	[O]
32	PREEMPTOR #2 ACTIVE	[O]
22	PREEMPTOR #3 ACTIVE	[O]
34	PREEMPTOR #4 ACTIVE	[O]
1	PREEMPTOR #5 ACTIVE	[O]
48	PREEMPTOR #6 ACTIVE	[O]
59	PREEMPT CMU INTERLOCK	[O]
15	PREEMPTOR FLASH CONTROL	[O]

```
      (1K PULL UP)                          [O]

27    COORD STATUS                          [O]
 5    CROSS STREET SYNC                     [O]

28    NIC SPECIAL FUNCTION 1                [O]
 8    NIC SPECIAL FUNCTION 2                [O]
24    NIC SPECIAL FUNCTION 3/               [O]
      SPARE OUTPUT 1                        [O]
11    NIC SPECIAL FUNCTION 4/               [O]
      SPARE OUTPUT 2                        [O]

41    SPARE OUTPUT 4                        [O]
45    SPARE OUTPUT 5                        [O]
51    SPARE OUTPUT 6                        [O]
52    SPARE OUTPUT 7                        [O]
54    SPARE OUTPUT 8                        [O]
```

Port 3B 25 pin Telemetry Connector

PIN	FUNCTION	I/O
3	SYSTEM DETECTOR A1	[I]
2	SYSTEM DETECTOR A2	[I]
5	SYSTEM DETECTOR B1	[I]
19	SYSTEM DETECTOR B2	[I]
4	SYSTEM DETECTOR C1	[I]
1	SYSTEM DETECTOR C2	[I]
7	SYSTEM DETECTOR D1	[I]
8	SYSTEM DETECTOR D2	[I]
18	LOCAL FLASH	[I]
20	CONFLICT FLASH	[I]
16	DOOR OPEN	[I]
(MAINTENANCE REQUIRED)		[I]
17	ALARM 1	[I]
21	ALARM 2	[I]
14	TLM SPARE 1	[I]
6	TLM SPARE 2	[I]
15	EXTERNAL ADDRESS ENABLE	[I]
24	RECEIVE 1	[O]
25	RECEIVE 2	[O]
12	TRANSMIT 1	[O]
13	TRANSMIT 2	[O]
9	TLM SPECIAL FUNCTION 1	[O]
22	TLM SPECIAL FUNCTION 2	[O]
10	TLM SPECIAL FUNCTION 3	[O]
23	TLM SPECIAL FUNCTION 4	[O]

PORT 1 SDLC

PIN	FUNCTION	I/O
1	Tx Data +	[O]
2	Logic Ground	[-]
3	Tx Clock +	[O]
4	Logic Ground	[-]
5	Rx Data +	[I]
6	Logic Ground	[-]
7	Rx Clock +	[I]
8	Logic Ground	[-]
9	Tx Data -	[O]
10	Port 1 Disable [I] (0VDC=disable)	
11	Tx Clock -	[O]
12	Chassis Ground	[-]
13	Rx Data -	[I]
14	Reserved	
15	Rx Clock -	[I]

Note: TX pins at the BIU are Rx pins at the controller.

Rx pins at the BIU are TX pins at the controller.

TYPE 1 POWER

PIN	FUNCTION	I/O
A	AC Neutral	[I]
B	Not Used	
C	AC Line	[I]
D	Not Used	
E	Not Used	
F	Fault Monitor	[O]
G	Logic Ground	[O]
H	Chassis Ground	[I]
I	Not Used	
J	Not Used	

PORT 2 Terminal

PIN	FUNCTION	I/O
1	Chassis Ground	[-]
2	Transmit Data	[O]
3	Receive Data	[I]
4	Request To Send	[O]
5	Clear To Send	[I]
6	Not Used	
7	Logic Ground	[-]
8	Data Carrier Det	[I]
9-19	Not Used	
20	Data Termnl Ready	[O]
21-25	Not Used	

PORT 3A EIA-232 Telemetry

PIN	FUNCTION	I/O
1	DXD	
2	RXD	
3	TXD	
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	NC	
9	NC	

PORT 3B 9-PIN Telemetry Connector

PIN	FUNCTION	I/O
1	Transmit 1	[O]
2	Transmit 2	[O]
3	Reserved	
4	Receive 1	[I]
5	Receive 2	[I]
6	Chassis Ground	[-]
7	Reserved	
8	Reserved	
9	Chassis Ground	[-]

Equipment	**170 Controller C1 Default Assignment Per Safetran Cabinet Standard**
Connectivity	**Controller Type ASC/3-RM (same as 2070 2A) with C1 Connector**

Pin # - Input	Safetran 332 (Base) ASC/3 2.43.10	Safetran 330 TBD	Safetran 336 TBD	Safetran 303 TBD	Safetran 337 TBD
Pin 39	VEHICLE DET 02				
Pin 40	VEHICLE DET 18				
Pin 41	VEHICLE DET 06				
Pin 42	VEHICLE DET 22				
Pin 43	VEHICLE DET 10				
Pin 44	VEHICLE DET 26				
Pin 45	VEHICLE DET 14				
Pin 46	VEHICLE DET 30				
Pin 47	VEHICLE DET 04				
Pin 48	VEHICLE DET 20				
Pin 49	VEHICLE DET 08				
Pin 50	VEHICLE DET 24				
Pin 51	PREEMPT CALL 1				
Pin 52	PREEMPT CALL 2				
Pin 53	MAN CONT ENA				
Pin 54	TEST A				
Pin 55	VEHICLE DET 17				
Pin 56	VEHICLE DET 01				
Pin 57	VEHICLE DET 21				
Pin 58	VEHICLE DET 05				
Pin 59	VEHICLE DET 25				
Pin 60	VEHICLE DET 09				
Pin 61	VEHICLE DET 29				
Pin 62	VEHICLE DET 13				
Pin 63	VEHICLE DET 03				
Pin 64	VEHICLE DET 19				
Pin 65	VEHICLE DET 07				
Pin 66	VEHICLE DET 23				
Pin 67	PED DET 02				
Pin 68	PED DET 06				
Pin 69	PED DET 04				
Pin 70	PED DET 08				
Pin 71	PREEMPT CALL 3				
Pin 72	PREEMPT CALL 4				
Pin 73	PREEMPT CALL 5				
Pin 74	PREEMPT CALL 6				
Pin 75	SPLIT DEMAND 1				
Pin 76	VEHICLE DET 11				
Pin 77	VEHICLE DET 27				
Pin 78	VEHICLE DET 15				
Pin 79	VEHICLE DET 31				

Pin # - Input	Safetran 332 (Base) ASC/3 2.43.10	Safetran 330 TBD	Safetran 336 TBD	Safetran 303 TBD	Safetran 337 TBD
Pin 80	INT ADV				
Pin 81	LOCAL FLASH				
Pin 82	STOP TIME				

Pin # - Output	Safetran 332 (Base) ASC/3 2.43.10	Safetran 330 TBD	Safetran 336 TBD	Safetran 303 TBD	Safetran 337 TBD
Pin 2	PH 4 DON'T WLK				
Pin 3	PH 4 WALK				
Pin 4	PH 4 RED				
Pin 5	Ph 4 YELLOW				
Pin 6	PH 4 GREEN				
Pin 7	Ph 3 RED				
Pin 8	PH 3 YELLOW				
Pin 9	Ph 3 GREEN				
Pin 10	PH 2 DON'T WLK				
Pin 11	PH 2 WALK				
Pin 12	PH 2 RED				
Pin 13	PH 2 YELLOW				
Pin 15	PH 2 GREEN				
Pin 16	PH 1 RED				
Pin 17	PH 1 YELLOW				
Pin 18	PH 1 GREEN				
Pin 19	PH 8 DON'T WLK				
Pin 20	PH 8 WALK				
Pin 21	PH 8 RED				
Pin 22	PH 8 YELLOW				
Pin 23	PH 8 GREEN				
Pin 24	PH 7 RED				
Pin 25	PH 7 YELLOW				
Pin 26	PH 7 GREEN				
Pin 27	PH 6 DON'T WLK				
Pin 28	PH 6 WALK				
Pin 29	PH 6 RED				
Pin 30	PH 6 YELLOW				
Pin 31	PH 6 GREEN				
Pin 32	PH 5 RED				
Pin 33	PH 5 YELLOW				
Pin 34	PH 5 GREEN				
Pin 35	OLA GREEN				
Pin 36	OLB GREEN				
Pin 37	OLA YELLOW				

Pin # - Output	Safetran 332 (Base) ASC/3 2.43.10	Safetran 330 TBD	Safetran 336 TBD	Safetran 303 TBD	Safetran 337 TBD
Pin 38	OVERLAP B YELLOW				
Pin 83	NIC SPEC FUNC 1				
Pin 84	NIC SPEC FUNC 3				
Pin 85	OLD RED				
Pin 86	OLD YELLOW				
Pin 87	OLD GREEN				
Pin 88	OLC RED				
Pin 89	OLC YELLOW				
Pin 90	OLC GREEN				
Pin 91	COORD FREE STAT				
Pin 93	CRD SYNC OUT				
Pin 94	OLB RED				
Pin 95	OLB YELLOW				
Pin 96	OLB GREEN				
Pin 97	OLA RED				
Pin 98	OLA YELLOW				
Pin 99	OLA GREEN				
Pin 100	NIC SPEC FUNC 2				
Pin 101	AUTOMATIC FLASH				
Pin 102	NIC SPEC FUNC 4				
Pin 103	WATCHDOG				

9. APPENDIX D: BILLS OF MATERIALS

Part No.	Description	Number of Pages
100-0000-501	Assy, ASC/3-1000, TS2 Type 1	1
100-0000-502	Assy, ASC/3-2100, TS2, Type 2	1
100-0000-508	Assy, ASC/3-1000, TS2, Slimline Enclosure	1
100-0000-509	Assy, ASC/3-2100, TS2, Slimline Enclosure	1
100-1013-501	Assy, PCB, ASC/3 Main 110V	15
100-1013-502	Assy, PCB, Main, 220V, ASC/3	1
100-1046-501	Assy, Kit, Ethernet, ASC/3	1
100-1084-501	Assy, ASC/3 Telemetry, 9-Pin, FSK Module	2
100-1084-502	Assy, ASC/3 Telemetry, 25-Pin, FSK Module	2
100-1084-503	Assy, ASC/3 Telemetry, 9-Pin, RS232 Module	2
100-1084-504	Assy, ASC/3 Telemetry, 25-Pin, RS232 Module	2

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-0000-501 -Rev. D
ASSY, ASC/3-1000,TS2
TYPE 1

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1035-003	D	ENCLOSURE, DIE-CASTING ASC/3	1	EA				
2	100-1030-501	F	ASSY,FRONT PANEL,TS2-1,ASC/	1	EA				
9	100-1025-001	B	COVER, ETHERNET, ASC/3	1	EA				
10	N238P9B	NC	HEX NUT/LK WSHR #4 STL/CAD	2	EA				
11	31144P1	K	IDENT PLATE CNTLR ECONOLITE	1	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-0000-502 -Rev. D
ASSY, ASC/3-2100, TS2
TYPE 2

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1035-003	D	ENCLOSURE, DIE-CASTING ASC/3	1	EA				
2	100-1030-502	E	ASSY,FRONT PANEL,TS2-2,ASC/	1	EA				
9	100-1025-001	B	COVER, ETHERNET, ASC/3	1	EA				
10	N238P9B	NC	HEX NUT/LK WSHR #4 STL/CAD	2	EA				
11	31144P1	K	IDENT PLATE CNTLR ECONOLITE	1	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-0000-508 -Rev. A
ASSY.ASC3-10000,TS2
SLIMLINE ENCLOSURE

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1065-001	A	ENCLOSURE,ASC/3,ALUMINUM	1	EA				
2	100-1030-501	F	ASSY,FRONT PANEL,TS2-1,ASC/	1	EA				
9	100-1025-001	B	COVER, ETHERNET, ASC/3	1	EA				
10	N238P9B	NC	HEX NUT/LK WSHR #4 STL/CAD	2	EA				
11	31144P1	K	IDENT PLATE CNTLR ECONOLITE	1	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-0000-509 -Rev. A
ASSY,ASC/3-2100,TS2
SLIMLINE ENCLOSURE

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1065-001	A	ENCLOSURE,ASC/3,ALUMINUM	1	EA				
2	100-1030-502	E	ASSY,FRONT PANEL,TS2-2,ASC/	1	EA				
9	100-1025-001	B	COVER, ETHERNET, ASC/3	1	EA				
10	N238P9B	NC	HEX NUT/LK WSHR #4 STL/CAD	2	EA				
11	31144P1	K	IDENT PLATE CNTLR ECONOLITE	1	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1013-001	C	PCB,MAIN CONT,ASC/3	1	EA				
2	33730P1	C	XSTR NPN 2222A	1	EA				
						Q3			
							MOTOROLA	MMBT2222ALT1	
3	32169P19	NC	CAPAC ELECT 18000MF 35V SNAP MTG	1	EA				
						C76			
							NICHICON	LLQ1V183MHSC	
							PANASONIC	ECO-S1VA183EA	
							PANASONIC	ECO-S1VP183DA	
4	1003-005	NC	CAPAC, 120uF, 50V RADIAL	1	EA				
						C15			
							PANASONIC	EEUFC1H121	
5	33740P5682	E	CAP,CE,50V,6800PF,10% SMT 0805 X7R	1	EA				
						C93			
							AVX	08055C682KAT2A	
							KEMET	C0805C682K5RAC	
							MURATA ERIE	GRM400805X7R682RK050AD	
							NIC	NMC0805X7R682K50TRP	
6	33748P0104	B	CAPAC .1MF 16V SMT 0603 X7R	84	EA				
						C2-13 C18 C20-75 C78-79 C84-85 C87-89 C92 C95-96 C99-100 C102-104			

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
							AVX	0603YC104KAT2A	
							NIC	NMC0603X7R104K16	
7	56668P3	E	CHOKE HASH 250MH	1	EA				
						L2			
							J.W.MILLER	5254	
							JEFFERS	10744-8	
8	31838P505	NC	HDR 5/10 CKT DUAL .100 PITCH,2 ROW	2	EA				
						J12-13			
							AMP	104350-5	
9	31369P26	K	CONN D SUB 15S W/W METAL	1	EA				
						J1			
							CINCH	DAKL-15SUT	
10	31369P27	K	CONN D SUB 25S W/W METAL	1	EA				
						J2			
							CINCH	DBKL-25SUT	
11	31369P25	L	CONN D SUB 9P METAL	1	EA				
						J3			
							CINCH	DEKL-9UTI	
12	58064P12	P	DIODE 1N4763A	1	EA				
						CR24			

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
							DIODES INC.	1N4763A	
							MOTOROLA	1N4763A	
13	31535P2	K	WAFER 3 CKT	1	EA				
						JP2			
							MOLEX	22-03-2031	
14	31535P1	K	WAFER 2 CKT	7	EA				
						JP1 JP3-8			
							MOLEX	22-03-2021	
15	33851P1	NC	DIODE MMBZ15VDLT1 ZENER SMT SOT23 COMMON CATHODE	12	EA				
						CR7-18			
							MOTOROLA	MMBZ15VDLT1	
16	33872P000	A	RES 0 5% 1/10W SMT SMT	6	EA				
						R25 R58 R60-61 R70-71			
							DALE/VISHAY	CRCW0603000J	
17	33872P152	B	RES 1.5K 5% 1/10W SMT SMT	7	EA				
						R1 R3-4 R6 R55-R57			
							DALE/VISHAY	CRCW0603152J	
							STACKPOLE	RMC 1/16 1.5K 5% R	
18	33872P103	A	RES 10K 5% 1/10W SMT SMT	21	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
						R22 R28 R47-54 R64 R74-75 R81 R83 R88-93			
							DALE/VISHAY	CRCW0603103J	
19	31263P97	I	RES 10K 3W 5% W/W REPLACES 0500-0039	2	EA				
						R7 R9			
							CLAROSTAT	VC3D-10K	
							DALE/VISHAY	CW2C-14-10K 5%	
							SAGE	1240S-10K 5%	
20	33711P121	C	RES 12O OHM 5% 1/4W SMT SMT	5	EA				
						R5 R29 R32 R36 R2			
							DALE/VISHAY	CRCW1206121JRT1	
							KOA SPEER	RM73B2BT121J	
21	54719P153	F	RES 22 MEG 1/4W 5% MIL-R-11F	1	EA				
						R10			
							DALE/VISHAY	CMF55-22M 1%T1 T/R	
22	1066-007	NC	RES,1/2W,7.5 OHM,5%	1	EA				
						R31			
							STACKPOLE	CF 1/2 7.5 5% R	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
23	33893P105	NC	TRANSORB SMBJ5.0C SMT	2	EA				
						CR5-6			
							GEN SEMI	SMBJ5.0C	
							RFE INTERNATIONAL	SMBJ5.0C	
24	33892P4	NC	DIODE BRIDGE DF04S SMT	4	EA				
						CR1-4			
							DIODES INC.	DF04S	
25	33748P5471	B	CAPAC 470PF 50V SMT SMT 0603 X7R	1	EA				
						C1			
							AVX	0603C471KAT2A	
							MURATA ERIE	06035C471KAT2A	
							MURATA ERIE	GRM39X7R471K050B	
							NIC	NMC0603X7R471K50	
27	33741P5104	K	CAP,CE,50V,.1MF,10% SMT 1206 X7R	1	EA				R
						C98			
							AVX	12065C104KAT2A	
							KEMET	C1206C104K5RAC	
28	33831P4	NC	DIODE MBR0520 20V 1/2A 1/2A,SMT CASE 403	3	EA				
						CR28-30			
							ON SEMICONDUCTOR	MBR0520LT1	
29	33870P1	A	DIODE FDLL4148 SMT D035	2	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
						CR31-32			
							NATIONAL SEMI	FDLL4148	
							PHILLIPS SEMI	PMLL4148	
30	33831P3	NC	DIODE MBR340 34V SMT CASE 403	5	EA				
						CR19-22 CR26			
							ON SEMICONDUCTOR	MBRS340T3	
31	33737P3	C	XTAL 32.768KHZ	1	EA				
						Y1			
							EPSON	MC-405-32.768K-A2	
							FOX	FSM327	
32	31769P61	K	TRANSZORB P6KE27A 600W	1	EA				
						CR25			
							DIODES INC.	P6KE27A	
							FAIRCHILD	P6KE27A	
							GEN SEMI	P6KE27A	
							GEN INSTRUMENTS	P6KE27A	
							MOTOROLA	P6KE27A	
							ST MICROELECTRONICS	P6KE27A	
33	1028-002	NC	TRANSORB,P6KE33AG,1Uaa,TH	1	EA				
						CR27			
							ON SEMICONDUCTOR	P6KE33AG	
34	31770P1	E	VARISTOR 55 JOULES 212V-255V METAL OXIDE	3	EA				
						RV1-3			

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
							AVX	VE17P00151K	
							GE/HARRIS	V150LA20B	
35	1041-002	NC	HEX SCHMITT-TRIGGER INVERTER	1	EA				
						U22			
							TEXAS INSTRUMENTS	SN74AHC14PWR	
36	1039-002	NC	OCTAL BUFFER/DRIVER 3 STATE OUTS 3.3V TSSOP	3	EA				
						U16 U19 U23			
							TEXAS INSTRUMENTS	SN74AHC244PWR	
37	1036-007	NC	IC, LOGIC, OCTAL BUS TRANSCVR W/3-ST OUT	1	EA				
						U14			
							TEXAS INSTRUMENTS	SN74AHC245PWR	
38	1036-003	NC	QUADRUPLE 2-INPUT POSITIVE AND GATE	1	EA				
						U24			
							TEXAS INSTRUMENTS	SN74ALVC08DR	
39	1038-002	NC	FULL DUPLEX RS-485 TRANSCEIVER	2	EA				
						U2-3			
							ANALOG DEVICES	ADM3491AR	
40	1040-001	NC	CMOS PRESETTABLE DIVIDE-BY-N COUNTER	1	EA				
						U18			
							TEXAS INSTRUMENTS	CD4018BNSR	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
41	1061-002	NC	RES NETWORK 10K	7	EA	R17-20 R23-24 R45	DALE/VISHAY	CRA12E1002103J	
42	1033-003	A	IC,STRATA-FLASH 8MB 3V	1	EA	U9	INTEL	TE28F640J3D-75	
43	1052-001	NC	XTAL OSC 7.372MHZ	1	EA	U21	FOX	F4100 7.372/JIT02-DC3AF	R
44	1095-002	NC	2MM 8 COND. RIBBON WIRE TRAP	1	EA	J5	MOLEX	052147-0810	
45	1094-011	NC	HEADER 8 COND.4.2MM	1	EA	J7	MOLEX	39-29-9082	
46	1094-021	NC	CONN 20 POS BRD TO BRD	2	EA	J4 J11	MOLEX	44245-0020	
47	1094-008	NC	HEADER 34 COND DUAL ROW 2 ROW	1	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
						J10			
							AMP	1-103186-7	
48	1094-009	NC	HEADER 40 COND DUAL ROW 2 ROW	1	EA				
						J9			
							AMP	HDR/40P/2-103186-0	
49	1095-003	NC	CONN HSG, 12 POS, PULL	1	EA				
						J8			
							MOLEX	052147-1210	
50	1094-010	NC	HEADER 6 COND.4.2MM 2 ROW	1	EA				
						J6			
							MOLEX	39-29-9062	
51	56671P49	NC	STDF,RND,4-40,.250,F,BRS,SWA	6	EA				
						XJ1-XJ3			
							UNICORP	SS244-1-C-7	
52	1025-004	NC	LED BI-COLOR	1	EA				
						LED2			
							LITE-ON	LTL-30EFJ	
53	1030-005	NC	HYSTERETIC PFET BUCK CONTROLLER	1	EA				
						U12			
							NATIONAL ELECTRIC	LM3485MM	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
54	1030-004	NC	IC RESET	1	EA	U20	NATIONAL SEMI	LM8364BALMF30	
55	1031-002	NC	PROCESSOR MPC862T	1	EA	U1	MOTOROLA	XPC862TZP50B	
56	1032-003	NC	MCU 16 BIT MSP430	1	EA	U11	TEXAS INSTRUMENTS	MSP43012221DW	
57	1033-005	NC	SDRAM 64 MB 32 BIT WIDE	1	EA	U6	MICRON	MT448LC2M32B2TG-7	
58	1060-001	NC	RES 2.49K 0603	14	EA	R11,R13-14,R26-27,R34-35,R39, R41-44,R59,R80	DALE/VISHAY	CRCW06032491FRT1	
59	1060-002	NC	RES 20.0K 0603	1	EA	R15	DALE/VISHAY	CRCW06032002FRT1	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
60	33872P243	NC	RES 24K 5% 1/10W SMT SMT	1	EA	R30	DALE/VISHAY	CRCW0603243J	
61	1060-003	NC	RES 33.2K 0603	3	EA	R16 R37 R40	DALE/VISHAY	CRCW06033322FRT1	
63	32289P1	H	JUMPER SHORTING	1	EA	XJP2	AMP CIRCUIT ASSEMBLY CIRCUIT ASSEMBLY	390088-2 CA-02SJC-B CA-02SJC-B BLUE	
64	1075-003	B	TRANSISTOR, P-CHNL LOGIC PWR TRENCH MOSFET	1	EA	Q1	VISHAY SILICONIX	Si4835BDY-T1-E3	R
65	1075-002	NC	N-CHANNEL PWR MOSFET	2	EA	Q2 Q4	ON SEMICONDUCTOR	BSS138LT1	
66	32911P21	NC	BATTERY, LITHIUM,3V,COIN CEL PC MOUNT	1	EA	B1	PANASONIC	VL2330-1VC	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
67	1049-001	NC	BRIDGE RECTIFIER	1	EA				
						CR23			
							DIODES INC.	DF08S	
68	1000-007	NC	CAP VARIABLE 3-10PF 0603	1	EA				
						C17			
							MURATA ERIE	TZB4Z100AB10R01	
69	1042-001	NC	IC MCT6 DUAL IOPTO ISOL J-LEAD SMT	1	EA				
						U10			
							FAIRCHILD	MCT6.S	
70	1050-016	A	INDUCTOR, 3.9uH,SURFACE MO	1	EA				
						L1			
							BUSSMAN	DR124-3R9-R	
							STACKPOLE	PCS124MT3R9	
							SUMIDA	CDRH124NP-3R9MC	
71	1050-006	NC	SURFACE MOUNT INDUCTOR	1	EA				
						L3			
							VISHAY	IDCP-3722-NB-821-20%	
72	1050-005	NC	INDUCTOR FERRITE BEAD	3	EA				
						FB1-FB3			
							VISHAY	ILHB1206RK121V	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
73	33872P330	NC	RES 33 OHM 1/10W 5% SMT SMT	2	EA	R79 R95	DALE/VISHAY	CRCW0603330J	
74	1065-001	NC	RES 2.2 OHMS 5W WW	2	EA	R76-77	DALE/VISHAY	CPSM-5 2R2 10%	
75	1038-001	A	RS232 TRANSCEIVER W/AUTO POWER DOWN	1	EA	U4	ST MICROELECTRONICS	ST3243ECDR	R
76	1036-005	NC	IC DUAL 4 BIT BINARY COUNTER SN74HC393PW	1	EA	U17	TEXAS INSTRUMENTS	SN74HC393PW	
77	1039-001	A	RS232 DRIVERS & RECEIVERS	1	EA	U5	ST MICROELECTRONICS	ST3222CDR	R
78	1033-012	A	IC,MEM,SRAM,4MB,512K X 8 45ns,SOIC-32	1	EA	U13	CYPRESS CYPRESS	CY62148DV30LL-55SXI CY62148EV30LL-45SXI	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
79	1031-001	NC	IC,TL16C 55O CFN, A SYNC COMMUNICATIONS	1	EA	U15	TEXAS INSTRUMENTS	TL16550CFN	
80	1000-001	NC	CAPAC .001 uF 50V 0603	1	EA	C16	AVX	06035C102KAT2Z	
81	1000-002	NC	CAPAC CE 10uF 0805 0805	2	EA	C19 C94	AVX	0805C106KAT2A	
83	33748P5101	NC	CAPAC 100 PF 0603 SMT 0603	1	EA	C101	AVX	06035C101KAT2A	
84	33740P5050	A	CAPAC 5 PF 50V 0805 0805	1	EA	C86	MURATA ERIE	GRM40COG050J050BD	
85	33872P102	A	RES,1/10W,1K,5%,0603 SMT	4	EA	R21 R46 R73 R84	DALE/VISHAY	CRCW0603102J	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-501 -Rev. P
ASSY, PCB, ASC/3 MAIN 110V

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
86	1036-032	NC	IC,LOGIC,74AHC1G32, SINGLE INPUT OR GATE,SOT23-5	1	EA	U25	TEXAS INSTRUMENTS	SN74AHC1G32DBV	R

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1013-502 -Rev. NC
ASSY,PCB,MAIN,220V,ASC/3

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1013-501	P	ASSY, PCB, ASC/3 MAIN 110V	1	EA				
2	31263P103	J	RES 33K 3W 5% W/W	2	EA				
						R7 R9			
							CALIFORNIA RESISTOR	SA31-3W-33K 5%	
							DALE/VISHAY	RS-5-33K-SW-5%	
							SAGE	1240S-33K 5%	
							SEI	WW5 33K 5% R	
3	31770P3	E	VARISTOR 75 JOULES 289V-430V METAL OXIDE	3	EA				
						RV1-3			
							GE/HARRIS	V275LA20A	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1046-501 -Rev. B
ASSY., KIT, ETHERNET, ASC/3

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1006-501	D	ASSY,PCB, ASC/3, ETHERNET	1	EA				
2	1208-009	NC	BRACKET,.343X.375,2X4-40, .062 STL,ZINC PLATE	2	EA				
3	1245-001	NC	SCREW-PAN HD.PH,NYLOCK, STL	2	EA		KEYSTONE	621	
4	100-1038-501	B	ASSY, RIBBON CABLE 40 PIN ASC/3	1	EA		KAD	0404MPPPA	
5	N404P11B	NC	WSHR LK INT #4 STL ZINC PLATED	2	EA				
6	MWI-09-151	NC	ASC/3 ETHERNET KIT ASSY,INS	0	REF				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-501 -Rev. A
ASSY,ASC/3 TELEMETRY,9 PIN
FSK MODULE

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1085-001	NC	PLATE,FRONT,TELEMETRY,D9 ASC/3	1	EA				
4	100-1091-501	NC	ASSY,PCB,TELEMETRY,CONN D ASC/3	1	EA				
5	100-1093-501	B	ASSY,PCB,TELEMETRY,MAIN,AS	1	EA				
6	31348P58	U	BLOCK LATCHING REAR PNL 2 PER PKG (.090 PNL)	1	PK				
8	33230P7	NC	SCREW,CAP PANEL,4-40 X.375,S	2	EA		AMP	747080-2	
9	1333-002	NC	RING,RETAINING,.187 X .015 EXTERNAL,SS	2	EA		RAF ELECTRONIC HARDW	378-S-26	
10	1208-014	NC	BRACKET,.343 X .375,4-40,STL ZINC PLATE	2	EA		ROTOR CLIP	E-9SS	
13	N80P9004C	NC	SCREW,PNH PH,4-40 X .250 STL	2	EA		KEYSTONE	612	
14	N44P9005C	NC	SCREW,FILH SLT,4-40 X .312 STL	3	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-501 -Rev. A
ASSY,ASC/3 TELEMETRY,9 PIN

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
15	N80P9003C	NC	SCRW #4 x 3/16 L PH PHIL STL	2	EA				
16	32289P1	H	JUMPER SHORTING	18	EA				
							AMP	390088-2	
							CIRCUIT ASSEMBLY	CA-02SJC-B	
							CIRCUIT ASSEMBLY	CA-02SJC-B BLUE	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-502 -Rev. A
ASSY,ASC/3 TELEMETRY,25 PIN
FSK MODULE

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1085-002	NC	PLATE,FRONT,TELEMETRY,D25 ASC/3	1	EA				
4	100-1092-501	A	ASSY,PCB,TELEMETRY,CONN D ASC/3	1	EA				
5	100-1093-501	B	ASSY,PCB,TELEMETRY,MAIN,AS	1	EA				
6	31348P12	U	SPRING LATCH KIT(9-37) 1 SET PER PKG	1	EA				
8	33230P7	NC	SCREW,CAP PANEL,4-40 X.375,S	2	EA		ITT CANNON	D110277	
9	1333-002	NC	RING,RETAINING,.187 X .015 EXTERNAL,SS	2	EA		RAF ELECTRONIC HARDW	378-S-26	
10	1208-014	NC	BRACKET,.343 X .375,4-40,STL ZINC PLATE	2	EA		ROTOR CLIP	E-9SS	
13	N80P9004C	NC	SCREW,PNH PH,4-40 X .250 STL	2	EA		KEYSTONE	612	
14	N44P9005C	NC	SCREW,FILH SLT,4-40 X .312 STL	1	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-502 -Rev. A
ASSY,ASC/3 TELEMETRY,25 PIN

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
15	N80P9003C	NC	SCREW,PNH PH,4-40 X .188 STL	2	EA				
16	32289P1	H	JUMPER SHORTING	18	EA				
							AMP	390088-2	
							CIRCUIT ASSEMBLY	CA-02SJC-B	
							CIRCUIT ASSEMBLY	CA-02SJC-B BLUE	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-503 -Rev. A
ASSY,ASC/3 TELEMETRY,9 PIN
RS232 MODULE

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1085-001	NC	PLATE,FRONT,TELEMETRY,D9 ASC/3	1	EA				
4	100-1091-501	NC	ASSY,PCB,TELEMETRY,CONN D ASC/3	1	EA				
5	100-1093-501	B	ASSY,PCB,TELEMETRY,MAIN,AS	1	EA				
6	31348P58	U	BLOCK LATCHING REAR PNL 2 PER PKG (.090 PNL)	1	PK				
8	33230P7	NC	SCREW,CAP PANEL,4-40 X.375,S	2	EA		AMP	747080-2	
9	1333-002	NC	RING,RETAINING,.187 X .015 EXTERNAL,SS	2	EA		RAF ELECTRONIC HARDW	378-S-26	
10	1208-014	NC	BRACKET,.343 X .375,4-40,STL ZINC PLATE	2	EA		ROTOR CLIP	E-9SS	
13	N80P9004C	NC	SCREW,PNH PH,4-40 X .250 STL	2	EA		KEYSTONE	612	
14	N44P9005C	NC	SCREW,FILH SLT,4-40 X .312 STL	3	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-503 -Rev. A
ASSY,ASC/3 TELEMETRY,9 PIN

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
15	N80P9003C	NC	SCRW #4 x 3/16 L PH PHIL STL	2	EA				
16	32289P1	H	JUMPER SHORTING	18	EA				
							AMP	390088-2	
							CIRCUIT ASSEMBLY	CA-02SJC-B	
							CIRCUIT ASSEMBLY	CA-02SJC-B BLUE	

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-504 -Rev. A
ASSY,ASC/3 TELEMETRY,25 PIN
RS232 MODULE

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
1	100-1085-002	NC	PLATE,FRONT,TELEMETRY,D25 ASC/3	1	EA				
4	100-1092-501	A	ASSY,PCB,TELEMETRY,CONN D ASC/3	1	EA				
5	100-1093-501	B	ASSY,PCB,TELEMETRY,MAIN,AS	1	EA				
6	31348P12	U	SPRING LATCH KIT(9-37) 1 SET PER PKG	1	EA				
8	33230P7	NC	SCREW,CAP PANEL,4-40 X.375,S	2	EA		ITT CANNON	D110277	
9	1333-002	NC	RING,RETAINING,.187 X .015 EXTERNAL,SS	2	EA		RAF ELECTRONIC HARDW	378-S-26	
10	1208-014	NC	BRACKET,.343 X .375,4-40,STL ZINC PLATE	2	EA		ROTOR CLIP	E-9SS	
13	N80P9004C	NC	SCREW,PNH PH,4-40 X .250 STL	2	EA		KEYSTONE	612	
14	N44P9005C	NC	SCREW,FILH SLT,4-40 X .312 STL	1	EA				

Single Level BOM Report

Econolite Control Products, Inc.

Production BOM No. 100-1084-504 -Rev. A
ASSY,ASC/3 TELEMETRY,25 PIN

Item	Part Number	Rev.	Description	Qty.	UOM	Reference Designator	Manufacturer	Manufacturer Part	Envir. Compl.
15	N80P9003C	NC	SCREW,PNH PH,4-40 X .188 STL	2	EA				
16	32289P1	H	JUMPER SHORTING	18	EA				
							AMP	390088-2	
							CIRCUIT ASSEMBLY	CA-02SJC-B	
							CIRCUIT ASSEMBLY	CA-02SJC-B BLUE	

10. APPENDIX E: SYSTEM INTERCONNECTION

A master transceiver can be interconnected with a number of local transceivers to make up a system. If a leased line is used for interconnection, up to 19 local transceivers can be connected. If customer-owned twisted pair lines are used, up to 24 local transceivers can be connected. Each transmitter output is essentially an open circuit unless it is ON. Each receiver has an input impedance of 15 kilohms.

The master transceiver can have either one or two Telemetry modules, allowing the system to be interconnected by either one or two data channels. For each channel, the master transmitter outputs are connected by a 2-wire command line that is connected to all local receiver inputs. The master receiver inputs and all local transmitter outputs are connected to another 2-wire read-back line. Transient protection on these lines is achieved with a Telemetry Interface Board (TIB) or a Communications Transient Suppressor (CTS) installed in the cabinets between each transceiver and the communication lines.

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11. APPENDIX F: LEASE-LINE INSTALLATION GUIDE

11.1. Introduction

Telephone Companies offer several types of networks designed for lease-line service. This guide is intended to assist Econolite system users and their local telephone company with installation of the proper data transmission lines required for Econolite systems.

Econolite recommends the **Broadcast Polling Multipoint Method** as a cost-effective and reliable means of networking traffic control equipment. "Polling" refers to the method in which a Master station addresses a particular local station anticipating a data response. Upon completion of the data transaction, the next local station is polled. Econolite utilizes this method but employs full duplex communications, whereby the Master station addresses the next local station while simultaneously receiving data from a previously addressed station.

The system consists of a single Master station, ASC/2M-1000 Zone Master or KMCE-10,000 Arterial Master and 1 to 24 local stations with any combination of the following controllers: ASC/3, ASC/2(S) family, the CBD, ASC-8000, ASC-8000RM, KMCE-8000, KFT-18/2400. All transmissions from the master station are simultaneously received by all local stations while all transmissions from local stations are received only by the master. Thus, the master station controls the network and no interaction between the local stations occurs.

The following specifications define telephone company lease-line requirements for Econolite Master/Local station networking. Econolite telemetry module modem design specifications are also enclosed to assist in telephone company circuit design. Further assistance from Econolite is available upon request.

Schematics and assembly drawings for the controller are listed below in the order that they appear in this chapter. These are subject to revision due to design changes made after the revision date of this manual. Contact Econolite if revised drawings are required.

11.2. Lease-Line Specification

Line Type:	Voice Grade
Interconnect Method:	Broadcast Polling Multipoint
Drops:	20 Points or 4,000 Facility Miles
Battery Voltage:	DC Voltage shall not be present on the line between tip and ring or tip, ring, and ground
Data Signal Power:	Maximum Transmitted: 0 dBm (3 second average) +13 dBm (instantaneous) Received: -16 dBm ±1 dB
Loss Variation:	No more than ±4 dB long term (12 dB to 20 dB) No more than ±3 dB short term
Terminal Equipment Impedance:	600 Ω ±10% resistive over the voiceband and balanced
Isolation To Ground:	At least 50 kΩ AC (300-3000 Hz)
Breakdown Voltage:	At least 1500 VRMS at 60 Hz
Channel Requirements:	Two channels minimum: (1) transmit, (1) receive. This is equivalent to one Econolite telemetry channel. For systems larger than 10 intersection controllers, Econolite recommends the use of two telemetry channels (four leased-lines) to ensure full data communications within 1 second.

11.3. Econolite Telemetry Module Modem Specifications

11.3.1. Transmitter Characteristics

Transmitter:	Digital-to-FSK modulator
Output Level:	0 dBm ±15% into a 600 Ω load adjustable to +6 dBm
Transmit Frequencies:	2200 Hz represents a digital LOW 1200 Hz represents a digital HIGH
Frequency Stability:	±1 Hz over the operating temperature range

11.3.2. Receiver Characteristics

Receiver:	FSK-to-digital demodulator
Signal-To-Noise: (In-band)	+10 dB or greater
Signal-To-60 Hz Noise:	Greater than -50 dB at an input signal level of 50 mV
Receiver Sensitivity	-34 dBm
Receiver Frequency:	2200 Hz represents a digital LOW 1200 Hz represents a digital HIGH
Common Mode Rejection (Input)	Greater than 40 dB

11.3.3. Data Channel Characteristics

Communication Line:	Unconditioned type 3002 voice grade, four-wire private line channel, or equivalent
Line Impedance:	600 Ω
Type of Transmission:	Time division multiplex/frequency shift keying
Baud Rate:	1200 bps
Word Length:	Eight bits plus odd vertical parity
Command Message:	Three words plus odd horizontal parity
Readback Message:	Two words plus odd horizontal parity with phantom address
Channel Capacity:	Twenty-five messages per second
Channel Operation:	One command message containing cycle, offset, split, master zero, and four special function commands is simultaneously transmitted to all local transceivers. Up to twenty-four command messages per second are then transmitted requesting status readbacks, data and special command and information.

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12. APPENDIX G: HW DIAGNOSTIC LOOPBACK CABLES

12.1. General Information

When performing the Auto-Loop diagnostic test that automatically cycles through all of the individual diagnostic tests in sequence, the ASC/3 controller power should be disconnected and all loopback cables should be installed before the Auto-Loop test is started. When performing individual tests that require a loopback cable, power should be disconnected before the loopback cable is installed.

The following tables describe the configuration of each of the individual ASC/3 controller loopback cables.

33279G1 ASC/3-2100 A Connector Loopback Cable

WIRE NO.	PREP ITEM	LENGTH (INCHES)	FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO TERM	TO FIT	REMARKS
1	1	8	PA	f	C	PA	s	C	26 WHT
2	1	8	PA	g	C	PA	Z	C	26 WHT
3	1	8	PA	h	C	PA	D	C	26 WHT
4	1	8	PA	N	C	PA	t	C	26 WHT
5	1	8	PA	EE	C	PA	a	C	26 WHT
6	1	8	PA	FF	C	PA	E	C	26 WHT
7	1	8	PA	w	C	PA	DD	C	26 WHT
8	1	8	PA	P	C	PA	u	C	26 WHT
9	1	8	PA	T	C	PA	CC	C	26 WHT-W/NEXT WIRE
10	1	8	PA	CC	C	PA	R	C	26 WHT-W/NEXT WIRE
11	1	8	PA	R	C	PA	AA	C	26 WHT
12	1	8	PA	S	C	PA	r	C	26 WHT-W/NEXT WIRE
13	1	8	PA	r	C	PA	k	C	26 WHT
14	1	8	PA	BB	C	PA	Y	C	26 WHT-W/NEXT WIRE
15	1	8	PA	Y	C	PA	j	C	26 WHT
16	1	8	PA	m	C	PA	X	C	26 WHT-W/NEXT WIRE
17	1	8	PA	X	C	PA	z	C	26 WHT
18	1	8	PA	K	C	PA	c	C	26 WHT
19	1	8	PA	L	C	PA	b	C	26 WHT
20	1	8	PA	M	C	PA	F	C	26 WHT
21	1	8	PA	n	C	PA	J	C	26 WHT
22	1	8	PA	v	C	PA	H	C	26 WHT
23	1	8	PA	i	C	PA	G	C	26 WHT
24	1	8	PA	x	C	PA	e	C	26 WHT
25	1	8	PA	GG	C	PA	d	C	26 WHT
26	1	8	PA	A	C	PA	q	C	26 WHT
27	1	8	PA	C	C	PA	HH	C	26 WHT-W/NEXT WIRE
28	1	8	PA	HH	C	PA	y	C	26 WHT
29	2	6	PWR	AC+	S	PA	p	C	20 BLK SPLICE W/PWR CORD BLK
30	3	6	PWR	AC-	S	PA	U	C	20 WHT SPLICE W/PWR CORD WHT
31	4	6	PWR	GND	S	PA	V	C	20 GRN SPLICE W/PWR CORD GRN

33279G2 ASC/3-2100 B Connector Loopback Cable

FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO TERM	TO FIT	REMARKS
PB	N	C	PB	D	C	W/NEXT WIRE
PB	D	C	PB	AA	C	
PB	P	C	PB	E	C	W/NEXT WIRE
PB	E	C	PB	p	C	
PB	i	C	PB	F	C	W/NEXT WIRE
PB	F	C	PB	q	C	
PB	R	C	PB	Y	C	W/NEXT WIRE
PB	Y	C	PB	FF	C	
PB	m	C	PB	Z	C	W/NEXT WIRE
PB	Z	C	PB	HH	C	W/NEXT WIRE
PB	HH	C	PB	T	C	W/NEXT WIRE
PB	T	C	PB	a	C	W/NEXT WIRE
PB	a	C	PB	DD	C	
PB	j	C	PB	s	C	W/NEXT WIRE
PB	s	C	PB	A	C	
PB	U	C	PB	r	C	
PB	V	C	PB	t	C	
PB	L	C	PB	b	C	W/NEXT WIRE
PB	b	C	PB	GG	C	
PB	M	C	PB	c	C	W/NEXT WIRE
PB	c	C	PB	BB	C	
PB	h	C	PB	G	C	W/NEXT WIRE
PB	G	C	PB	CC	C	
PB	g	C	PB	d	C	W/NEXT WIRE
PB	d	C	PB	w	C	
PB	n	C	PB	H	C	W/NEXT WIRE
PB	H	C	PB	EE	C	W/NEXT WIRE
PB	EE	C	PB	k	C	W/NEXT WIRE
PB	k	C	PB	J	C	W/NEXT WIRE
PB	J	C	PB	u	C	
PB	x	C	PB	e	C	W/NEXT WIRE
PB	e	C	PB	C	C	
PB	S	C	PB	K	C	
PB	z	C	PB	f	C	W/NEXT WIRE
PB	f	C	PB	B	C	W/NEXT WIRE
PB	B	C	PB	W	C	W/NEXT WIRE
PB	W	C	PB	X	C	W/NEXT WIRE
PB	X	C	PB	v	C	W/NEXT WIRE
PB	v	C	PB	y	C	

33279G3 ASC/3-2100 C Connector Loopback Cable

WIRE NO.	DESCRIPTION OF WIRE	LENGTH (INCHES)	FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO TERM	TO FIT	REMARKS
1	26 AWG WHT	8	PC	P	C	PC	i	C	W/NEXT WIRE
2	26 AWG WHT	8	PC	i	C	PC	K	C	W/NEXT WIRE
3	26 AWG WHT	8	PC	K	C	PC	M	C	
4	26 AWG WHT	8	PC	R	C	PC	J	C	W/NEXT WIRE
5	26 AWG WHT	8	PC	J	C	PC	L	C	W/NEXT WIRE
6	26 AWG WHT	8	PC	L	C	PC	DD	C	
7	26 AWG WHT	8	PC	m	C	PC	H	C	W/NEXT WIRE
8	26 AWG WHT	8	PC	H	C	PC	N	C	
9	26 AWG WHT	8	PC	n	C	PC	j	C	W/NEXT WIRE
10	26 AWG WHT	8	PC	j	C	PC	k	C	
11	26 AWG WHT	8	PC	a	C	PC	PP	C	
12	26 AWG WHT	8	PC	u	C	PC	HH	C	
13	26 AWG WHT	8	PC	v	C	PC	A	C	
14	26 AWG WHT	8	PC	Z	C	PC	B	C	
15	26 AWG WHT	8	PC	Y	C	PC	c	C	
16	26 AWG WHT	8	PC	S	C	PC	g	C	W/NEXT WIRE
17	26 AWG WHT	8	PC	g	C	PC	AA	C	
18	26 AWG WHT	8	PC	T	C	PC	h	C	W/NEXT WIRE
19	26 AWG WHT	8	PC	h	C	PC	z	C	
20	26 AWG WHT	8	PC	p	C	PC	G	C	W/NEXT WIRE
21	26 AWG WHT	8	PC	G	C	PC	CC	C	
22	26 AWG WHT	8	PC	q	C	PC	LL	C	W/NEXT WIRE
23	26 AWG WHT	8	PC	LL	C	PC	BB	C	
24	26 AWG WHT	8	PC	V	C	PC	f	C	W/NEXT WIRE
25	26 AWG WHT	8	PC	f	C	PC	KK	C	
26	26 AWG WHT	8	PC	U	C	PC	E	C	W/NEXT WIRE
27	26 AWG WHT	8	PC	E	C	PC	y	C	
28	26 AWG WHT	8	PC	EE	C	PC	F	C	W/NEXT WIRE
29	26 AWG WHT	8	PC	F	C	PC	NN	C	
30	26 AWG WHT	8	PC	r	C	PC	JJ	C	W/NEXT WIRE
31	26 AWG WHT	8	PC	JJ	C	PC	MM	C	
32	26 AWG WHT	8	PC	t	C	PC	x	C	W/NEXT WIRE
33	26 AWG WHT	8	PC	x	C	PC	w	C	
34	26 AWG WHT	8	PC	W	C	PC	e	C	W/NEXT WIRE
35	26 AWG WHT	8	PC	e	C	PC	C	C	
36	26 AWG WHT	8	PC	X	C	PC	D	C	W/NEXT WIRE
37	26 AWG WHT	8	PC	D	C	PC	GG	C	
38	26 AWG WHT	8	PC	s	C	PC	d	C	W/NEXT WIRE
39	26 AWG WHT	8	PC	d	C	PC	FF	C	W/NEXT WIRE
40	26 AWG WHT	8	PC	FF	C	PC	b	C	

33279G4 ASC/3-2100 D Connector Loopback Cable

WIRE NO.	DESCRIPTION OF WIRE	LENGTH (INCHES)	FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO TERM	TO FIT	REMARKS
1	26 AWG WHT	8	D	1	C	D	57	C	
2	26 AWG WHT	8	D	2	C	D	50	C	
3	26 AWG WHT	8	D	5	C	D	60	C	W/NEXT WIRE
4	26 AWG WHT	8	D	60	C	D	49	C	
5	26 AWG WHT	8	D	8	C	D	61	C	
6	26 AWG WHT	8	D	11	C	D	55	C	
7	26 AWG WHT	8	D	15	C	D	56	C	
8	26 AWG WHT	8	D	21	C	D	58	C	
9	26 AWG WHT	8	D	22	C	D	9	C	
10	26 AWG WHT	8	D	23	C	D	38	C	
11	26 AWG WHT	8	D	24	C	D	3	C	
12	26 AWG WHT	8	D	27	C	D	12	C	
13	26 AWG WHT	8	D	28	C	D	36	C	
14	26 AWG WHT	8	D	29	C	D	10	C	
15	26 AWG WHT	8	D	32	C	D	6	C	
16	26 AWG WHT	8	D	33	C	D	4	C	
17	26 AWG WHT	8	D	34	C	D	47	C	
18	26 AWG WHT	8	D	41	C	D	20	C	
19	26 AWG WHT	8	D	42	C	D	13	C	
20	26 AWG WHT	8	D	43	C	D	16	C	
21	26 AWG WHT	8	D	44	C	D	14	C	
22	26 AWG WHT	8	D	45	C	D	19	C	
23	26 AWG WHT	8	D	46	C	D	18	C	
24	26 AWG WHT	8	D	48	C	D	17	C	
25	26 AWG WHT	8	D	51	C	D	25	C	
26	26 AWG WHT	8	D	52	C	D	30	C	
27	26 AWG WHT	8	D	53	C	D	26	C	W/NEXT WIRE
28	26 AWG WHT	8	D	26	C	D	40	C	
29	26 AWG WHT	8	D	54	C	D	31	C	W/NEXT WIRE
30	26 AWG WHT	8	D	31	C	D	35	C	
31	26 AWG WHT	8	D	59	C	D	37	C	W/NEXT WIRE
32	26 AWG WHT	8	D	37	C	D	39	C	

33279G5 25 pin FSK Loopback Diagnostic Cable

WIRE NO.	DESCRIPTION OF WIRE	LENGTH (INCHES)	FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO TERM	TO FIT	REMARKS
1	26 AWG WHT	8	P3	9	C	P3	3	C	W/NEXT WIRE
2	26 AWG WHT	8	P3	3	C	P3	4	C	W/NEXT WIRE
3	26 AWG WHT	8	P3	4	C	P3	14	C	W/NEXT WIRE
4	26 AWG WHT	8	P3	14	C	P3	15	C	
5	26 AWG WHT	8	P3	22	C	P3	2	C	W/NEXT WIRE
6	26 AWG WHT	8	P3	2	C	P3	1	C	W/NEXT WIRE
7	26 AWG WHT	8	P3	1	C	P3	17	C	W/NEXT WIRE
8	26 AWG WHT	8	P3	17	C	P3	20	C	
9	26 AWG WHT	8	P3	10	C	P3	5	C	W/NEXT WIRE
10	26 AWG WHT	8	P3	5	C	P3	7	C	W/NEXT WIRE
11	26 AWG WHT	8	P3	7	C	P3	21	C	W/NEXT WIRE
12	26 AWG WHT	8	P3	21	C	P3	18	C	
13	26 AWG WHT	8	P3	23	C	P3	19	C	W/NEXT WIRE
14	26 AWG WHT	8	P3	19	C	P3	8	C	W/NEXT WIRE
15	26 AWG WHT	8	P3	8	C	P3	6	C	W/NEXT WIRE
16	26 AWG WHT	8	P3	6	C	P3	16	C	
17			R1	1	S	R3	1	S	INSTALL ASSY IN CONN
18			R1	2	S	R4	1	S	INSTALL ASSY IN CONN
19			R2	1	S	R3	2	S	INSTALL ASSY IN CONN
20			R2	2	S	R4	2	S	INSTALL ASSY IN CONN
21	26 AWG WHT	8	R3	2	S	P3	12	C	TRANSMIT 1
22	26 AWG WHT	8	R4	2	S	P3	13	C	TRANSMIT 2
23	26 AWG WHT	8	R3	1	S	P3	24	C	RECEIVE 1
24	26 AWG WHT	8	R4	1	S	P3	25	C	RECEIVE 2

33279G6 9 pin FSK Loopback Cable

WIRE NO.	DESCRIPTION OF WIRE	LENGTH (INCHES)	FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO FIT	TO FIT
1	26 AWG WHT	8	P7	1	C	P7	4	C
2	26 AWG WHT	8	P7	2	C	P7	5	C

33279G7 15 pin SDLC Loopback Cable

WIRE NO.	DESCRIPTION OF WIRE	LENGTH (INCHES)	FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO TERM	TO FIT
1	26 AWG WHT	8	P5	1	C	P5	5	C
2	26 AWG WHT	8	P5	3	C	P5	7	C
3	26 AWG WHT	8	P5	9	C	P5	13	C
4	26 AWG WHT	8	P5	11	C	P5	15	C

33279G8 25 pin Port 2 Loopback Cable

1	26 AWG WHT	6.5	P2	2	C	P2	3	C	TXD/RXD
2	26 AWG WHT	6.5	P2	4	C	P2	5	C	RTS/CTS
3	26 AWG WHT	6.5	P2	20	C	P2	6	C	DTR/DSR-TO NEXT WIRE
4	26 AWG WHT	6.5	P2	6	C	P2	8	C	DSR/DCD

100-1044-501 Port 3A test cable

33279G10 Telemetry Interface

WIRE NO.	DESCRIPTION OF WIRE	LENGTH (INCHES)	FROM ITEM	FROM TERM	FROM FIT	TO ITEM	TO TERM	TO FIT
1	26 AWG WHT	8	P1	1	C	P1	7	C
2	26 AWG WHT	8	P1	2	C	P1	3	C

Ethernet Crossover Cable

Wire No.	From P1	To P2
1	1	3
2	2	6
3	3	1
4	4	2
5	5	4
6	6	5
7	7	7
8	8	8

32864G1 ASC-2S/1000 Power Cable

ITEM #	WIRE	LENGTH "	FROM/TERM	TO/TERM
1	18 AWG GRN	6	P1-H	P1-SHL
2	PWR CORD 18 AWG 3 COND	72	P1-C	PWR-BLK (AC+)
3	PWR CORD 18 AWG 3 COND	72	P1-A	PWR-WHT (AC-)
4	PWR CORD 18 AWG 3 COND	72	P1-H	PWR-GRN (CG)

13. APPENDIX H: TS1 SUITCASE DIAGNOSTIC TESTING

13.1. General Information

The TS1 Suitcase test allows the user to verify if controller inputs (as supplied by the suitcase tester) are operating correctly. Each input from the suitcase tester will display as an “X” if asserted, and displays a “.” (period) when not asserted. The display position of the input under test is determined by the address of the input

The display positions are organized in bytes, so the top line of display positions will display inputs 0x00 to 0x1F, the next line down will display inputs 0x20 to 0x3F, etc.

This test has no specific pass/fail criteria since it is intended for use as a troubles-shooting tool only.

SCREEN HD-D

```
                TS1 SUITCASE TEST
Inputs
0123........ ........ ........ ........
4567........ ........ ........ ........
89AB........ ........ ........ ........
C   ........ ........ ........ ........

Outputs
0123........ ........ ........ ........
4567........ ........ ........ ........
89AB........ ........ ........ ........
CDE ........ ........ ........ ........
    01234567 01234567 01234567 01234567

          PRESS ANY KEY TO RETURN
```

ASC/3 TS2 I/O ADDRESS TABLE on	Type	I/O Address	Connector Designation.
Phase 2 Vehicle Detector	[I]	0x00	A-K
Phase 2 Pedestrian Detector	[I]	0x01	A-L
Stop Time (Ring 1)	[I]	0x02	A-N
Inhibit Max Term (Ring 1)	[I]	0x03	A-P
External Start	[I]	0x04	A-R
Interval Advance	[I]	0x05	A-S
Indicator Lamp Control	[I]	0x06	A-T
Phase 1 Vehicle Detector	[I]	0x07	A-f
Phase 1 Pedestrian Detector	[I]	0x08	A-g
Force Off (Ring 1)	[I]	0x09	A-i
Min Recall All Phases	[I]	0x0A	A-j
Manual Control Enable	[I]	0x0B	A-k
Call To Non-Actuated I	[I]	0x0C	A-m
Test Input A	[I]	0x0D	A-n
Omit All-Red Clear (Ring 1)	[I]	0x0E	A-w
Red Rest (Ring 1)	[I]	0x0F	A-x
I/O Mode Bit A	[I]	0x10	A-q
I/O Mode Bit B	[I]	0x11	A-y
I/O Mode Bit C	[I]	0x12	A-HH
Call To Non-Actuated II	[I]	0x13	A-z
Test Input B	[I]	0x14	A-AA
Walk Rest Modifier	[I]	0x15	A-BB
Pedestrian Recycle (Ring 1)	[I]	0x16	A-FF
Max II Selection (Ring 1)	[I]	0x17	A-GG
Phase 2 Hold	[I]	0x18	A-M
Phase 1 Hold	[I]	0x19	A-h

ASC/3 TS2 I/O ADDRESS TABLE on	Type	I/O Address	Connector Designation.
Phase 2 Ped Omit	[I]	0x1A	A-v
Phase 1 Ped Omit	[I]	0x1B	A-EE
Phase 3 Omit	[I]	0x1C	B-R
Phase 2 Omit	[I]	0x1D	B-S
Phase 5 Ped Omit	[I]	0x1E	B-T
Phase 1 Omit	[I]	0x1F	B-U
Preempt 2 Detector	[I]	0x20	B-B
Phase 4 Vehicle Detector	[I]	0x21	B-L
Phase 4 Pedestrian Detector	[I]	0x22	B-M
Phase 3 Vehicle Detector	[I]	0x23	B-N
Phase 3 Pedestrian Detector	[I]	0x24	B-P
Ped Recycle (Ring 2)	[I]	0x25	B-V
Preempt 4 Detector	[I]	0x26	B-W
Preempt 5 Detector	[I]	0x27	B-X
Phase 4 Omit	[I]	0x28	B-g
Phase 4 Hold	[I]	0x29	B-h
Phase 3 Hold	[I]	0x2A	B-i
Phase 3 Ped Omit	[I]	0x2B	B-j
Phase 6 Ped Omit	[I]	0x2C	B-k
Phase 7 Ped Omit	[I]	0x2D	B-m
Phase 8 Ped Omit	[I]	0x2E	B-n
Phase 4 Ped Omit	[I]	0x2F	B-x
Preempt 6 Detector	[I]	0x30	B-v
Free (no coord)	[I]	0x31	B-y
Max II Selection (Ring 2)	[I]	0x32	B-z
Phase 5 Vehicle Detector	[I]	0x33	C-P
Phase 5 Pedestrian Detector	[I]	0x34	C-R
Phase 6 Vehicle Detector	[I]	0x35	C-S
Phase 6 Pedestrian Detector	[I]	0x36	C-T
Phase 7 Pedestrian Detector	[I]	0x37	C-U
Phase 7 Vehicle Detector	[I]	0x38	C-V
Phase 8 Pedestrian Detector	[I]	0x39	C-W
Force Off (Ring 2)	[I]	0x3A	C-Y
Stop Timing (Ring 2)	[I]	0x3B	C-Z
Inhibit Max Term (Ring 2)	[I]	0x3C	C-a
Test Input C	[I]	0x3D	C-b
Phase 8 Vehicle Detector	[I]	0x3E	C-t
Red Rest Mode (Ring 2)	[I]	0x3F	C-u
Phase 8 Hold	[I]	0x40	C-X
Phase 5 Hold	[I]	0x41	C-m
Phase 5 Omit	[I]	0x42	C-n
Phase 6 Hold	[I]	0x43	C-p
Phase 6 Omit	[I]	0x44	C-q
Phase 7 Omit	[I]	0x45	C-r
Phase 8 Omit	[I]	0x46	C-s
Phase 7 Hold	[I]	0x47	C-EE
Omit Red Clear (Ring 2)	[I]	0x48	C-v

ASC/3 TS2 I/O ADDRESS TABLE on	Type	I/O Address	Connector Designation.
Split Demand	[I]	0x49	D-3
System Command Coord Sync	[I]	0x4A	D-4
System Command Cycle Bit 3	[I]	0x4B	D-6
System Command Split Bit 2	[I]	0x4C	D-9
System Command Offset Bit 2	[I]	0x4D	D-10
System Command Offset Bit 1	[I]	0x4E	D-12
Expanded Detector #8	[I]	0x4F	D-13
Time Reset	[I]	0x50	D-14
System Command Split Bit 1	[I]	0x51	D-16
Expanded Detector #1	[I]	0x52	D-17
Expanded Detector #4	[I]	0x53	D-18
Test Input E	[I]	0x54	D-19
Test Input C	[I]	0x55	D-20
System Command Cycle Bit 1	[I]	0x56	D-25
Coord Free	[I]	0x57	D-26
Expanded Detector #5	[I]	0x58	D-30
Expanded Detector #3	[I]	0x59	D-31
System Command Cycle Bit 2	[I]	0x5A	D-35
System Command Offset Bit 3	[I]	0x5B	D-36
Test Input D	[I]	0x5C	D-37
Dual Coord	[I]	0x5D	D-38
Expanded Detector #6	[I]	0x5E	D-39
Expanded Detector #7	[I]	0x5F	D-40
Expanded Detector #2	[I]	0x60	D-47
Preemptor Call #2	[I]	0x61	D-49
Preemptor Call #3. Bus #1	[I]	0x62	D-50
Preemptor Call #4. Bus #2	[I]	0x63	D-55
Preemptor Call #5. Bus #3	[I]	0x64	D-56
Preemptor Call #1	[I]	0x65	D-57
CMU Stop Time (Conflict Flash)	[I]	0x66	D-58
Remote Flash	[I]	0x67	D-60
Preemptor Call #6. Bus #4	[I]	0x68	D-61
Not Assigned	[n/a]		D-7
Phase 1 Red	[O]	0x00	A-D
Phase 1 Don't Walk	[O]	0x01	A-E
Phase 2 Red	[O]	0x02	A-F
Phase 2 Don't Walk	[O]	0x03	A-G
Phase 2 Ped Clear	[O]	0x04	A-H
Phase 2 Walk	[O]	0x05	A-J
Flashing Logic Out	[O]	0x06	A-X
Status Bit C (Ring 1)	[O]	0x07	A-Y
Phase 1 Yellow	[O]	0x08	A-Z
Phase 1 Ped Clear	[O]	0x09	A-a
Phase 2 Yellow	[O]	0x0A	A-b
Phase 2 Green	[O]	0x0B	A-c
Status Bit B (Ring 1)	[O]	0x0C	A-r
Phase 1 Green	[O]	0x0D	A-s

ASC/3 TS2 I/O ADDRESS TABLE on	Type	I/O Address	Connector Designation.
Phase 1 Walk	[O]	0x0E	A-t
Coded Status Bit A (Ring 1)	[O]	0x0F	A-CC
Phase 3 Green	[O]	0x10	B-D
Phase 3 Yellow	[O]	0x11	B-E
Phase 3 Red	[O]	0x12	B-F
Phase 4 Red	[O]	0x13	B-G
Phase 4 Ped Clear	[O]	0x14	B-H
Phase 4 Don't Walk	[O]	0x15	B-J
Phase 3 Walk	[O]	0x16	B-Y
Phase 3 Ped Clear	[O]	0x17	B-Z
Phase 2 Check	[O]	0x18	A-d
Phase 2 On	[O]	0x19	A-e
Phase 1 Check	[O]	0x1A	A-u
Phase 1 On	[O]	0x1B	A-DD
Phase 1 Next	[O]	0x1C	B-A
Phase 2 Next	[O]	0x1D	B-C
Phase 4 Check	[O]	0x1E	B-K
Phase 4 On	[O]	0x1F	B-e
Phase 3 Don't Walk	[O]	0x20	B-a
Phase 4 Green	[O]	0x21	B-b
Phase 4 Yellow	[O]	0x22	B-c
Phase 4 Walk	[O]	0x23	B-d
Overlap A Yellow	[O]	0x24	B-p
Overlap A Red	[O]	0x25	B-q
Overlap D Red	[O]	0x26	B-u
Overlap D Green	[O]	0x27	B-w
Overlap A Green	[O]	0x28	B-AA
Overlap B Yellow	[O]	0x29	B-BB
Overlap B Red	[O]	0x2A	B-CC
Overlap C Red	[O]	0x2B	B-DD
Overlap D Yellow	[O]	0x2C	B-EE
Overlap C Green	[O]	0x2D	B-FF
Overlap B Green	[O]	0x2E	B-GG
Overlap C Yellow	[O]	0x2F	B-HH
Status Bit A (Ring 2)	[O]	0x30	C-A
Status Bit B (Ring 2)	[O]	0x31	C-B
Phase 8 Don't Walk	[O]	0x32	C-C
Phase 8 Red	[O]	0x33	C-D
Phase 7 Yellow	[O]	0x34	C-E
Phase 7 Red	[O]	0x35	C-F
Phase 6 Red	[O]	0x36	C-G
Phase 5 Red	[O]	0x37	C-H
Phase 4 Next	[O]	0x38	B-f
Phase 3 Check	[O]	0x39	B-r
Phase 3 On	[O]	0x3A	B-s
Phase 3 Next	[O]	0x3B	B-t
Phase 5 Next	[O]	0x3C	C-M

ASC/3 TS2 I/O ADDRESS TABLE on	Type	I/O Address	Connector Designation.
Phase 5 On	[O]	0x3D	C-N
Phase 5 Check	[O]	0x3E	C-k
Phase 6 Check	[O]	0x3F	C-BB
Phase 5 Yellow	[O]	0x40	C-J
Phase 5 Ped Clear	[O]	0x41	C-K
Phase 5 Don't Walk	[O]	0x42	C-L
Status Bit C (Ring 2)	[O]	0x43	C-c
Phase 8 Walk	[O]	0x44	C-d
Phase 8 Yellow	[O]	0x45	C-e
Phase 7 Green	[O]	0x46	C-f
Phase 6 Green	[O]	0x47	C-g
Phase 6 On	[O]	0x48	C-CC
Phase 6 Next	[O]	0x49	C-DD
Phase 8 Check	[O]	0x4A	C-FF
Phase 8 On	[O]	0x4B	C-GG
Phase 8 Next	[O]	0x4C	C-HH
Phase 7 Check	[O]	0x4D	C-MM
Phase 7 On	[O]	0x4E	C-NN
Phase 7 Next	[O]	0x4F	C-PP
Phase 6 Yellow	[O]	0x50	C-h
Phase 5 Green	[O]	0x51	C-i
Phase 5 Walk	[O]	0x52	C-j
Phase 8 Ped Clear	[O]	0x53	C-w
Phase 8 Green	[O]	0x54	C-x
Phase 7 Don't Walk	[O]	0x55	C-y
Phase 6 Don't Walk	[O]	0x56	C-z
Phase 6 Ped Clear	[O]	0x57	C-AA
Phase 7 Walk	[O]	0x58	C-JJ
Phase 7 Ped Clear	[O]	0x59	C-KK
Phase 6 Walk	[O]	0x5A	C-LL
Premptor #5 Active	[O]	0x5B	D-1
System Command Offset Bit 3	[O]	0x5C	D-2
Cross Street Sync	[O]	0x5D	D-5
NIC Special Function #2	[O]	0x5E	D-8
NIC Special Function #4/Spare #2	[O]	0x5F	D-11
Preemptor Flash Control	[O]	0x60	D-15
System Command Split Bit 1	[O]	0x61	D-21
Premptor #3 Active	[O]	0x62	D-22
Premptor #1 Active	[O]	0x63	D-23
NIC Special Function #3/Spare #1	[O]	0x64	D-24
Coord Status	[O]	0x65	D-27
NIC Special Function #1	[O]	0x66	D-28
System Command Cycle Bit 3	[O]	0x67	D-29
Premptor #2 Active	[O]	0x68	D-32
System Command Offset Bit 1	[O]	0x69	D-33
Premptor #4 Active	[O]	0x6A	D-34
Spare Output 4	[O]	0x6B	D-41

ASC/3 TS2 I/O ADDRESS TABLE on	Type	I/O Address	Connector Designation.
System Command Offset Bit 2	[O]	0x6C	D-42
System Command Cycle Bit 1	[O]	0x6D	D-43
System Command Cycle Bit 2	[O]	0x6E	D-44
Spare Output 5	[O]	0x6F	D-45
System Command Split Bit 2	[O]	0x70	D-46
Premptor #6 Active	[O]	0x71	D-48
Spare Output 6	[O]	0x72	D-51
Spare Output 7	[O]	0x73	D-52
System Command Sync Output	[O]	0x74	D-53
Spare Output 8	[O]	0x75	D-54
Preempt CMU Interlock (1K pullup)	[O]	0x76	D-59
Voltage Monitor	[O]		A-C
Fault Monitor	[O]		A-A